General Description

The PCI Express (PCIe) DO-254 Certifiable Data Package is made up of the artifacts produced by applying the DO-254 lifecycle to the Xilinx® PCIe IP and an encrypted version of the source code. This includes the following completed documents:

- Plan for Hardware Aspects of Certification
- Hardware Validation and Verification Plan
- Hardware Configuration Management Plan
- Hardware Design Plan
- Hardware Process Assurance Plan
- Hardware Validation and Verification Standard
- Hardware Requirements Standard
- Hardware Design Standard
- Hardware Requirements Document
- Hardware Design Document
- Hardware Configuration Index
- Verification Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
- Hardware Test Procedures
- Hardware Verification Results
- Hardware Elemental Analysis Results
- Hardware Requirements Traceability Matrix
- Hardware Accomplishment Summary

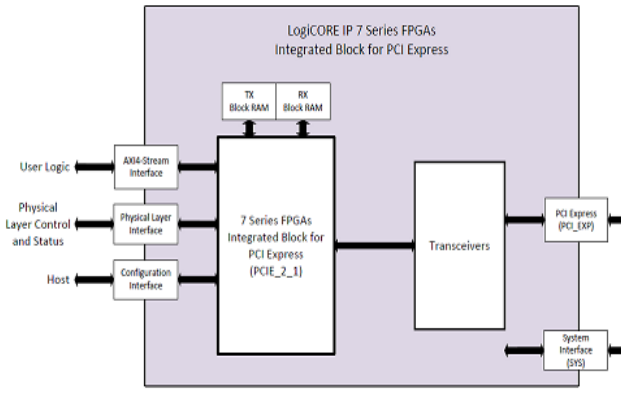
The above documents are available for certification efforts, however not all documents are included in the delivery package.

The DO-254 PCIe is a high-performance, highly flexible, scalable, and reliable, general purpose I/O core. This core incorporates Xilinx® Smart-IP technology to guarantee critical timing. This DO-254 PCIe core will support 1-lane and 2-lane Endpoint configurations at up to 5 Gb/s speeds. The core includes other non-programmable features such as 8B/10B encode and decode, as well as supports a maximum transaction payload of up to 128 byte.

Features

- Compliant with PCI Express Base Specification, rev. 2.1
- 1 lane or 2 lane operation
- Supports lane reversal and lane polarity inversion
- AXI-Stream user interface
- Custom Vendor ID
- Custom Device ID
- Custom Revision ID
- Custom Subsystem Vendor ID
- Custom Subsystem ID
- Supports 1 or 2 BARs (both customizable sizes)
- Configurable acceptable latency
- Supports enabling/disabling Virtual Channels

Block Diagram



Parameter Name	Allowable Values
C_EP_L0S_ACCPT_LAT	0-7
C_EP_L1_ACCPT_LAT	0-7
C_VC_ENABLED	“TRUE”, “FALSE”
C_DEVICE_TYPE	“ARTIX", “KINTEX”, “VIRTEX”,”ZYNQL”,”ZYNQM”
C_GEN_SPEED	“2.5G”, “5G”

Supported FPGA Families

Xilinx® 7-Series FPGA Families

Development Tools

ModelSim® v10.4 or later
Xilinx® Vivado® 2016.1 or later

Configuration

The DO-254 PCIe IP is configurable as shown below:

Parameter Name	Allowable Values
C_VEN_ID	0-FFFF
C_DEV_ID	0-FFFF
C_REV_ID	0-FF
C_SUBSYS_VEN_ID	0-FFFF
C_SUBSYS_ID	0-FFFF
C_BAR0	Defined by PCIe
C_BAR1	Defined by PCIe

Assumptions

Assumption 1: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system/safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.

Assumption 2: The objectives, activities and lifecycle data related specifically to the DO-254 PCIe IP will be provided to the Integrator for inclusion into their overall certification package.

Assumption 3: Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

Assumption 4: All objectives related to the building, integration and production (including Production Testing — ATP) of the system/LRU will be the responsibility of the integrator.

Assumption 5: Objectives related to hardware components other than the DO-254 PCIe IP are the responsibility of the integrator.

Assumption 6: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 PCIe IP in their system.

Assumption 7: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 PCIe IP.

Assumption 8: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 PCIe IP into their system.

Assumption 9: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System/Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 PCIe IP at the system level.

Assumption 10: The integrator is required to include a clock timing constraint for this DO-254 PCIe IP. This clock timing constraint will define the clock rate at which the IP core will operate. It is recommended that the integrator defines this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An example UCF file will be provided in Chapter 3 of the 10136-UG, but it is for reference only.

Assumption 11: The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results indicate that all configurations required to attain 100% coverage are tested.

Assumption 12: Some testing of the DO-254 PCIe IP was done on a test board, the integrator is responsible for complete IP black box testing in their system to verify that the IP performs its intended function in the system. In order to assist the integrator with determining what should be tested at the system level, Logicircuit has included a list of potential target tests in the “Potential Target Test” section of the User Guide for each IP. The integrator should evaluate the list of tests against the hardware functions of the IP they are using in their system to determine which tests they should perform at the system level.

Revision History

Revision	Reason/Description	Date	Subversion repository revision
-	Draft 1 has been formally released as Rev. -	8/9/2017	107