

General Description

The LMB BRAM Interface Controller) DO-254 Certifiable Data Package is made up of the artifacts produced by applying the DO-254 lifecycle to the Xilinx® LMB IP and an encrypted version of the source code. This includes the following completed documents:

- Plan for Hardware Aspects of Certification
- Hardware Validation and Verification Plan
- Hardware Configuration Management Plan
- Hardware Design Plan
- Hardware Process Assurance Plan
- Hardware Validation and Verification Standard
- Hardware Requirements Standard
- Hardware Design Standard
- Hardware Requirements Document
- Hardware Design Document
- Hardware Elemental Analysis Results
- Hardware Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
- Hardware Test Procedures
- Hardware Verification Results
- Hardware Elemental Analysis Results
- Hardware Requirements Traceability Matrix
- Hardware Accomplishment Summary

The DO-254 LMB BRAM Interface Controller provides LMB bus interfaces with byte enable support and is used in conjunction with the bram_block peripheral to provide a fast BRAM memory solution for MicroBlaze™ ILMB and DLMB ports. The LMB BRAM Interface Controller also supports byte, half-word, and word transfers and optional BRAM error correction and detection.

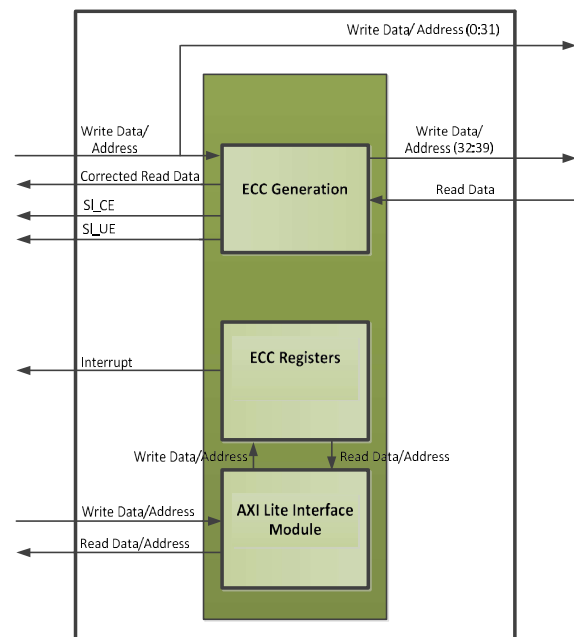
Safety Features

- Optional BRAM error correction and detection
- Single and double bit error detection
- Single bit error correction

Features

- LMB bus interface with byte enable support
- Byte, half-word, and word transfers
- AXI4 Lite Register Interface for ECC logic operation

Block Diagram



Configuration

Settable Parameter	Label in GUI
C_HIGHADDR	LMB BRAM Base Address
C_BASEADDR	LMB BRAM High Address
C_MASK	LMB Address Decode Mask
C_LMB_AWIDTH	LMB Address Bus Width
C_LMB_DWIDTH	LMB Address Data Bus Width
C_ECC	Error Correction Code
C_INTERCONNECT	Select Interconnect
C_FAULT_INJECT	Fault Inject Registers
C_CE_FAILING_REGISTERS	Correctable Error First Failing Register
C_UE_FAILING_REGISTERS	Uncorrectable Error First Failing Register
C_ECC_STATUS_REGISTERS	ECC Status and Control Register
C_ECC_ONOFF_REGISTER	ECC On/Off Register
C_ECC_ONOFF_RESET_VALUE	ECC On/Off Reset Value
C_CE_COUNTER_WIDTH	Correctable Error Counter Register Width
C_WRITE_ACCESS	Write Access setting
C_S_AXI_CTRL_DATA_WIDTH	S_AXI_CTRL Data Width
C_S_AXI_CTRL_ADDR_WIDTH	S_AXI_CTRL Address Width
C_S_AXI_CTRL_PROTOCOL	S_AXI_CTRL Protocol

Supported FPGA Families

Xilinx® 7-Series and Spartan®-6

Assumptions

Assumption 1: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system/safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU. The objectives, activities and lifecycle data related specifically to the DO-254 LMB BRAM Interface Controller IP Core 1.00a will be provided to the Integrator for inclusion into their overall certification package.

Assumption 2: Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

Assumption 3: Logicircuit will coordinate with the Certification Authority related only to DO-254 compliance with the DO-254 LMB BRAM Interface Controller IP Core 1.00a.

Assumption 4: All objectives related to the building, integration and Production (including Production Testing - ATP) of the system/LRU will be the responsibility of the integrator.

Assumption 5: Objectives related to hardware components other than the DO-254 LMB BRAM Interface Controller IP Core 1.00a are the responsibility of the integrator.

Assumption 6: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 LMB BRAM Interface Controller IP Core 1.00a in their system.

Assumption 7: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 LMB BRAM Interface Controller IP Core 1.00a.

Assumption 8: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 LMB BRAM Interface Controller IP Core 1.00a into their system.

Assumption 9: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System/Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 LMB BRAM Interface Controller IP Core 1.00a at the system level.

Assumption 10: The integrator is required to include a clock timing constraint for this DO-254 LMB IP Core 1.00a. This clock timing constraint will define the clock rate at which the IP core will operate. It is recommended that the integrator define this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An

example UCF file will be provided in 10115-UG, but it is for reference only.

Assumption 11: The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results will indicate that all configurations required to attain 100% coverage are tested.

Simulation validation for the DO-254 LMB IP Core 1.00a is being done on a test board. The integrator must revalidate a portion of this simulation on the integrator's target. Logiccircuit will provide the files and data necessary to perform this revalidation in 10115-UG.

In order to accomplish this revalidation, the integrator is required to design his PCB to have access to at least 20 spare FPGA pins that can be connected to a logic analyzer.

If the integrator chooses to do post place and route simulation on their system as an additional validation (again, this would only be a portion of Logiccircuit's simulation), Logiccircuit will provide the necessary files for the DO-254 LMB IP Core 1.00a.
