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| **8/8/2013, Rev. -** | microblaze  **DO-254 Distributed Memory 1.00a**  **Certifiable Data Package (DAL A)** |

**General Description**

The Distributed Memory Generator DO-254 Certifiable Data Package is made up of the artifacts produced by applying the DO-254 lifecycle to the Xilinx® Distributed Memory Generator IP v8.0 and an encrypted version of the source code. This includes the following completed documents:

* Plan for Hardware Aspects of Certification
* Hardware Validation and Verification Plan
* Hardware Configuration Management Plan
* Hardware Design Plan
* Hardware Process Assurance Plan
* Hardware Validation and Verification Standard
* Hardware Requirements Standard
* Hardware Design Standard
* Hardware Requirements Document
* Hardware Design Document
* Hardware Elemental Analysis Results
* Hardware Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
* Hardware Test Procedures
* Hardware Verification Results
* Hardware Elemental Analysis Results
* Hardware Requirements Traceability Matrix
* Hardware Accomplishment Summary

The above documents are available for certification efforts, however not all documents are included in the delivery package.

The DO-254 Distributed Memory Generator IP Core 1.00a, created and designed by Logicircuit, is used to create memory structures including Distributed ROM, Distributed Single-Port RAM,

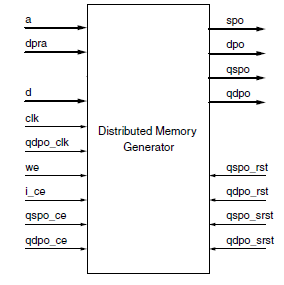
Distributed Dual-Port RAM, and Distributed Simple Dual-Port RAM.

This version of the DO-254 Distributed Memory Generator IP 1.00a does not have any built-in safety features.

**Features**

* Generates read-only memories (ROMs), single, simple dual, and dual-port random access memories (RAMs)
* Supports data depths ranging from 16–65,536 words
* Supports data widths ranging from 1–1024 bits
* Optional registered inputs and outputs
* Optional pipelining when output is registered

**I/O Overview**



**Supported FPGA Families**

Xilinx® 7-Series and Spartan®-6

**Development Tools**

Xilinx® ISE/EDK® 14.4 or later

ModelSim® v10.2a or later

Xilinx® ISIM 14.4 or later

Xilinx® XST 14.4 or later

Precision Synthesis 2012b or later

**Configuration**

The DO-254 Distributed Memory Generator version 1.00a is configurable as shown below:

| **Settable Parameter** | **Definition** |
| --- | --- |
| C\_FAMILY | Specifies the FPGA family being used |
| C\_ADDR\_WIDTH | Specifies the width of the address bus |
| C\_DEFAULT\_DATA | Specifies the value to which memory will be initialized to by default |
| C\_DEPTH | Specifies the depth of the generated memory |
| C\_HAS\_CLK | Specifies if the current configuration has a clock |
| C\_HAS\_D | Specifies if there is data input port |
| C\_HAS\_DPO | Specifies if there is a non-registered dual-port output bus |
| C\_HAS\_DPRA | Specifies if there is a dual/simple dual-port Read Address input |
| C\_HAS\_I\_CE | Species if there is an Input Clock Enable port |
| C\_HAS\_QDPO | Specifies if there is a registered dual/simple dual-port output bus |
| C\_HAS\_QDPO\_CE | Specifies if there is a registered dual/simple dual-port Clock Enable input |
| C\_HAS\_QDPO\_CLK | Specifies if there is a dual/simple dual-port clock input |
| C\_HAS\_QDPO\_RST | Specifies if there is a dual/simple dual-port registered output asynchronous reset |
| C\_HAS\_QDPO\_SRST | Specifies if there is a dual-port registered output synchronous reset |
| C\_HAS\_QSPO | Specifies if there is a registered single-port output bus |
| C\_HAS\_QSPO\_CE | Specifies if there is a registered single-port Clock Enable input |
| C\_HAS\_QSPO\_RST | Specifies if there is a single-port registered output asynchronous reset |
| C\_HAS\_QSPO\_SRST | Specifies if there is a single-port registered output synchronous reset |
| C\_HAS\_SPO | Specifies if there is a non-registered single-port output bus |
| C\_HAS\_WE | Specifies if there is a write enable |
| C\_MEM\_INIT\_FILE | Specifies the name of the MIF used for memory initialization |
| C\_ELABORATION\_DIR | Specifies the path to the MIF passed into “c\_mem\_init\_file" |
| C\_MEM\_TYPE | Specifies the type memory being implemented |
| C\_PIPELINE\_STAGES | Specifies the number of pipelines stages on the data output |
| C\_QCE\_JOINED | Specifies if both output ports share a common clock enable |
| C\_QUALIFY\_WE | Specifies if the write enable ("WE") is qualified by the "I\_CE" input where |
| C\_READ\_MIF | Specifies if the initialization file should be used |
| C\_REG\_A\_D\_INPUTS | Specifies if "D", "WE", and "A" are registered |
| C\_REG\_DPRA\_INPUT | Specifies if "DPRA" input is registered |
| C\_SYNC\_ENABLE | Specifies whether the synchronous output resets are qualified by the output clock enables or not |
| C\_WIDTH | Specifies the width of the input data port(s) |

**Assumptions**

**Assumption 1**: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system/safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.

The objectives, activities and lifecycle data related specifically to the DO-254 Distributed Memory Generator Core will be provided to the Integrator for inclusion into their overall certification package.

**Assumption 2**: Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

**Assumption 3**: All objectives related to the building, integration and production (including Production Testing — ATP) of the system/LRU will be the responsibility of the integrator.

**Assumption 4**: Objectives related to hardware components other than the DO-254 Distributed Memory Generator Core are the responsibility of the integrator.

**Assumption 5**: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 Distributed Memory Generator Core in their system.

**Assumption 6**: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 Distributed Memory Generator Core.

**Assumption 7**: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 Distributed Memory Generator Core into their system.

**Assumption 8**: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System/Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 Distributed Memory Generator Core at the system level.

**Assumption 9**: The integrator is required to include a clock timing constraint for this DO-254 Distributed Memory Generator Core. This clock timing constraint will define the clock rate at which the IP core will operate. It is recommended that the integrator defines this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An example UCF file will be provided in Chapter 3 of the 10125-UG, but it is for reference only.

**Assumption 10**: The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results indicate that all configurations required to attain 100% coverage are tested.