**General Description**

The AXI Serial Peripheral Interface (SPI) DO-254 Certifiable Data Package is made up of the artifacts produced by applying the DO-254 lifecycle to the Xilinx® AXI Serial Peripheral Interface IP v1.02.a and an encrypted version of the source code. This includes the following completed documents:

* Plan for Hardware Aspects of Certification
* Hardware Validation and Verification Plan
* Hardware Configuration Management Plan
* Hardware Design Plan
* Hardware Process Assurance Plan
* Hardware Validation and Verification Standard
* Hardware Requirements Standard
* Hardware Design Standard
* Hardware Requirements Document
* Hardware Design Document
* Hardware Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
* Verification Configuration Index
* Hardware Test Procedures
* Hardware Verification Results
* Hardware Elemental Analysis Results
* Hardware Requirements Traceability Matrix
* Hardware Accomplishment Summary

The above documents are available for certification efforts, however not all documents are included in the delivery package.

The DO-254 AXI SPI IP Core 1.00a, created and designed by Logicircuit, provides a serial interface to SPI devices such as SPI Electrically

Erasable Programmable Read-Only Memories (EEPROMs) and SPI serial flash devices.

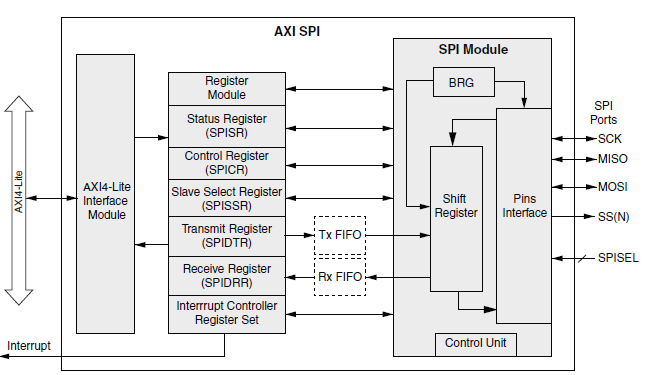
This version of the DO-254 AXI SPI IP includes the following built-in safety features:

* Contention Error Detection/Avoidance
* Underrun Detection
* Overrun Detection

**Features**

* AXI4-Lite interface is based on the AXI4 specification
* Connects as a 32-bit AXI4-Lite slave
* Supports four signal interfaces:
  + Master Out Slave In (MOSI)
  + Master In Slave Out (MISO)
  + Serial Clock (SC)
  + SS
* Slave select (SS) bit for each slave on the SPI bus
* Full-duplex operation
* Master and slave SPI modes
* Programmable clock phase and polarity
* Continuous transfer mode for automatic scanning of a peripheral
* Back-to-back transactions
* Automatic or manual slave select modes
* MSB/LSB first transactions
* Transfer length of 8-bits, 16-bits or 32-bits
* Local loopback capability for testing
* Multiple master and multiple slave environment
* Optional 16 element deep (an element is a byte, a half-word or a word) transmit and receive First In First Out (FIFO)

**Block Diagram**



**Supported FPGA Families**

Xilinx® 7-Series and Spartan®-6

**Development Tools**

Xilinx® ISE/EDK® 14.3 or later

ModelSim® v10.2a or later

Xilinx® ISIM 14.3 or later

Xilinx® XST 14.3 or later

**Configuration**

The DO-254 AXI SPI version 1.00a is configurable as shown below:

| **Settable Parameter** | **Definition** |
| --- | --- |
| C\_FAMILY | Specifies the FPGA family being used |
| C\_BASEADDR | Specifies the 32-bit AXI Base Address |
| C\_HIGHADDR | Specifies the 32-bit AXI High Address |
| C\_S\_AXI\_ADDR\_WIDTH | Specifies the AXI address bus width |
| C\_S\_AXI\_DATA\_WIDTH | Specifies the AXI data bus width |
| C\_FIFO\_EXIST | Specifies whether FIFOs are implemented |
| C\_SCK\_RATIO | Specifies the SPI clock frequency ratio |
| C\_NUM\_SS\_BITS | Specifies the total number of slave select bits |
| C\_NUM\_TRANSFER\_BITS | Specifies the number of bits transferred per transaction |

**Assumptions**

**Assumption 1**: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system/safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.

**Assumption 2**: The objectives, activities and lifecycle data related specifically to the DO-254 AXI SPI Core will be provided to the Integrator for inclusion into their overall certification package.

**Assumption 3**: Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

**Assumption 4**: All objectives related to the building, integration and production (including Production Testing — ATP) of the system/LRU will be the responsibility of the integrator.

**Assumption 5**: Objectives related to hardware components other than the DO-254 AXI SPI Core are the responsibility of the integrator.

**Assumption 6**: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 AXI SPI Core in their system.

**Assumption 7**: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 AXI SPI Core.

**Assumption 8**: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 AXI SPI Core into their system.

**Assumption 9**: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System/Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 AXI SPI Core at the system level.

**Assumption 10**: The integrator is required to include a clock timing constraint for this DO-254 AXI SPI Core. This clock timing constraint will define the clock rate at which the IP core will operate. It is recommended that the integrator defines this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An example UCF file will be provided in Chapter 3 of the 10130-UG, but it is for reference only.

**Assumption 11**: The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results indicate that all configurations required to attain 100% coverage are tested.

**Assumption 12**: Some testing of the DO-254 AXI SPI Core was done on a test board, the integrator is responsible for complete IP black box testing in his system. ***In order to accomplish this black box testing, the integrator is recommended to design his PCB to have access to at least XX (number defined in 10130-UG) spare FPGA pins that can be connected to a logic analyzer.***If the integrator chooses to do post place and route simulation on their system as an additional validation, Logicircuit will provide the necessary files for the DO-254 AXI SPI Core.

Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| Revision | Reason/Description | Date | Subversion repository revision |
| - | Draft 3 has been formally released as Rev. - | 10/17/2013 | 129 |
|  |  |  |  |