General Description

The AXI External Memory Controller (EMC) DO-254 Certifiable Data Package is made up of the artifacts produced by applying the DO-254 lifecycle to the Xilinx® AXI EMC IP and an encrypted version of the source code. This includes the following completed documents:

- Plan for Hardware Aspects of Certification
- Hardware Validation and Verification Plan
- Hardware Configuration Management Plan
- Hardware Design Plan
- Hardware Process Assurance Plan
- Hardware Validation and Verification Standard
- Hardware Requirements Standard
- Hardware Design Standard
- Hardware Requirements Document
- Hardware Design Document
- Hardware Elemental Analysis Results
- Hardware Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
- Hardware Test Procedures
- Hardware Verification Results
- Hardware Elemental Analysis Results
- Hardware Requirements Traceability Matrix
- Hardware Accomplishment Summary

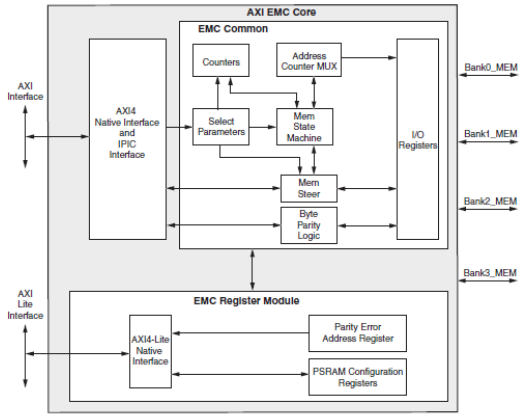
The above documents are available for certification efforts, however not all documents are included in the delivery package.

The AXI External Memory Controller (EMC) core provides an interface for external memory devices. The adaptable block provides memory controller functionality for SRAM, NOR Flash, and PSRAM/CellularRAM memory devices. The core provides an AXI4 Slave Interface that can be connected to AXI4 Master or Interconnect devices in the AXI4 Systems.

Features

- Supports AXI4 Slave Memory Map interface data width of 32 and 64 bits
- Supports AXI4 increment and wrap Transactions
- Supports AXI4 narrow and unaligned Transfers
- Supports up to four external memory banks
- Supports Synchronous SRAMs with
- configurable byte parity check and pipeline stages
- Supported memory types
    - Synchronous SRAM
    - Asynchronous SRAM
    - Linear Flash (or Parallel NOR Flash)
    - PSRAM (or Cellular RAM)
    - Page Mode NOR Flash
    - Numonyx Flash
- Provides configuration registers to dynamically change access mechanism for PSRAM and Numonyx Flash memories
- Provides Parity error status register for Synchronous SRAM memories

Block Diagram



Supported FPGA Families

Xilinx® 7-Series and Spartan®-6 Series

Development Tools

Xilinx® ISE/EDK® 14.5 or later
ModelSim® v10.2c or later (models required)
Xilinx® ISIM 14.5 or later (no models required)
Xilinx® XST 14.5 or later
Precision Synthesis 2012b or later

Configuration

The DO-254 LMB version 1.00a is configurable as shown below:

Settable Parameter	Label in GUI
C_AXI_CLK_PERIOD_PS	Period of Linear FLASH for burst mode
C_LINEAR_FLASH_SYNC_BURST	FLASH Synchronous Burst Mode
C_S_AXI_EN_REG	AXI Register Interface Enable
C_S_AXI_MEM_DATA_WIDTH	AXI Memory Interface Data Width
C_S_AXI_MEM_ID_WIDTH	AXI Memory Interface ID Width
C_S_AXI_MEM0_BASEADDR	Base Address of Bank 0
C_S_AXI_MEM0_HIGHADDR	High Address of Bank 0
C_S_AXI_MEM1_BASEADDR	Base Address of Bank 1
C_S_AXI_MEM1_HIGHADDR	High Address of Bank 1
C_S_AXI_MEM2_BASEADDR	Base Address of Bank 2
C_S_AXI_MEM2_HIGHADDR	High Address of Bank 2
C_S_AXI_MEM3_BASEADDR	Base Address of Bank 3
C_S_AXI_MEM3_HIGHADDR	High Address of Bank 3
C_INCLUDE_NEGEDGE_IOREGS	Include negative edge IO registers
C_NUM_BANKS_MEM	Number of Banks
C_MEM0_TYPE	Memory type for Bank 0
C_MEM1_TYPE	Memory type for Bank 1
C_MEM2_TYPE	Memory type for Bank 2

Settable Parameter	Label in GUI
C_MEM3_TYPE	Memory type for Bank 3
C_MEM0_WIDTH	Data Bus Width of Bank 0
C_MEM1_WIDTH	Data Bus Width of Bank 1
C_MEM2_WIDTH	Data Bus Width of Bank 2
C_MEM3_WIDTH	Data Bus Width of Bank 3
C_MAX_MEM_WIDTH	Maximum data bus width of all memory banks
C_PARITY_TYPE_MEM_0	Type of parity of BANK 0
C_PARITY_TYPE_MEM_1	Type of parity of BANK 1
C_PARITY_TYPE_MEM_2	Type of parity of BANK 2
C_PARITY_TYPE_MEM_3	Type of parity of BANK 3
C_INCLUDE_DATAWIDTH_MATCHING_0	Execute Multiple Memory Accesses to Match Bank 0 Data Bus Width to AXI Data Bus Width
C_INCLUDE_DATAWIDTH_MATCHING_1	Execute Multiple Memory Accesses to Match Bank 1 Data Bus Width to AXI Data Bus Width
C_INCLUDE_DATAWIDTH_MATCHING_2	Execute Multiple Memory Accesses to Match Bank 2 Data Bus Width to AXI Data Bus Width
C_INCLUDE_DATAWIDTH_MATCHING_3	Execute Multiple Memory Accesses to Match Bank 3 Data Bus Width to AXI Data Bus Width
C_SYNCH_PIPEDELAY_0	Pipeline Latency of Bank 0
C_TCEDV_PS_MEM_0	TCEDV of Bank 0
C_TAVDV_PS_MEM_0	TAVDV of Bank 0
C_TPACC_PS_FLASH_0	TPACC of Bank 0
C_THZCE_PS_MEM_0	THZCE of Bank 0
C_THZOE_PS_MEM_0	THZOE of Bank 0
C_TWC_PS_MEM_0	TWC of Bank 0
C_TWP_PS_MEM_0	TWP of Bank 0
C_TWPH_PS_MEM_0	TWPH of Bank 0
C_TLZWE_PS_MEM_0	TLZWE of Bank 0

Settable Parameter	Label in GUI
C_WR_REC_TIME_MEM_0	Write Recovery of Bank 0
C_SYNCH_PIPEDELAY_1	Pipeline Latency of Bank 1
C_TCEDV_PS_MEM_1	TCEDV of Bank 1
C_TAVDV_PS_MEM_1	TAVDV of Bank 1
C_TPACC_PS_FLASH_1	TPACC of Bank 1
C_THZCE_PS_MEM_1	THZCE of Bank 1
C_THZOE_PS_MEM_1	THZOE of Bank 1
C_TWC_PS_MEM_1	TWC of Bank 1
C_TWP_PS_MEM_1	TWP of Bank 1
C_TWPH_PS_MEM_1	TWPH of Bank 1
C_TLZWE_PS_MEM_1	TLZWE of Bank 1
C_WR_REC_TIME_MEM_1	Write Recovery of Bank 1
C_SYNCH_PIPEDELAY_2	Pipeline Latency of Bank 2
C_TCEDV_PS_MEM_2	TCEDV of Bank 2
C_TAVDV_PS_MEM_2	TAVDV of Bank 2
C_TPACC_PS_FLASH_2	TPACC of Bank 2
C_THZCE_PS_MEM_2	THZCE of Bank 2
C_THZOE_PS_MEM_2	THZOE of Bank 2
C_TWC_PS_MEM_2	TWC of Bank 2
C_TWP_PS_MEM_2	TWP of Bank 2
C_TWPH_PS_MEM_2	TWPH of Bank 2

Settable Parameter	Label in GUI
C_TLZWE_PS_MEM_2	TLZWE of Bank 2
C_WR_REC_TIME_MEM_2	Write Recovery of Bank 2
C_SYNCH_PIPEDELAY_3	Pipeline Latency of Bank 3
C_TCEDV_PS_MEM_3	TCEDV of Bank 3
C_TAVDV_PS_MEM_3	TAVDV of Bank 3
C_TPACC_PS_FLASH_3	TPACC of Bank 3
C_THZCE_PS_MEM_3	THZCE of Bank 3
C_THZOE_PS_MEM_3	THZOE of Bank 3
C_TWC_PS_MEM_3	TWC of Bank 3
C_TWP_PS_MEM_3	TWP of Bank 3
C_TWPH_PS_MEM_3	TWPH of Bank 3
C_TLZWE_PS_MEM_3	TLZWE of Bank 3
C_WR_REC_TIME_MEM_3	Write Recovery of Bank 3
C_S_AXI_REG_ADDR_WIDTH	AXI Register Interface Address Width
C_S_AXI_REG_DATA_WIDTH	AXI Register Interface Data Width

Supported FPGA Families

Xilinx® 7-Series and Spartan®-6

Development Tools

Xilinx® ISE/EDK® 14.5 or later
ModelSim® v10.2c or later (models required)
Xilinx® ISIM 14.5 or later (no models required)
Xilinx® XST 14.5 or later
Precision Synthesis 2012b or later

Assumptions

Assumption 1: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system / safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.
The objectives, activities and lifecycle data related specifically to the DO-254 AXI EMC IP Core will be provided to the Integrator for inclusion into their overall certification package.

Assumption 2: Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

Assumption 3: Logicircuit will coordinate with the Certification Authority related only to DO-254 compliance with the DO-254 AXI EMC IP Core.

Assumption 4: All objectives related to the building, integration and Production (including Production Testing - ATP) of the system/LRU will be the responsibility of the integrator.

Assumption 5: Objectives related to hardware components other than the DO-254 AXI EMC IP Core are the responsibility of the integrator.

Assumption 6: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 AXI EMC IP Core in their system.

Assumption 7: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 AXI EMC IP Core.

Assumption 8: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 AXI EMC IP Core into their system.

Assumption 9: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System / Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 AXI EMC IP Core at the system level.

Assumption 10: The integrator is required to include a clock timing constraint for this DO-254 AXI EMC IP core. This clock timing constraint will define the clock rate at which the IP core will operate. It is recommended that the integrator define this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An

example UCF file will be provided in 10117-UG, but it is for reference only.

Assumption 11: The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results will indicate that all configurations required to attain 100% coverage are tested.
Simulation validation for the DO-254 AXI EMC 1.00a is being done on a test board. The integrator must revalidate a portion of this simulation on the integrator's target. Logicircuit will provide the files and data necessary to perform this revalidation in 10117-UG.
In order to accomplish this revalidation, the integrator is required to design his PCB to have access to at least 13 spare FPGA pins that can be connected to a logic analyzer.
If the integrator chooses to do post place and route simulation on their system as an additional validation (again, this would only be a portion of Logicircuit's simulation), Logicircuit will provide the necessary files for the DO-254 AXI EMC IP.

Revision History

Revision	Reason/Description	Date	Subversion repository revision
-	Initial Release	9/2/2014	147