LOGICIRCUIT

MicroBlaze

DO-254 Tri-Mode Ethernet MAC v1.00a

12/6/2016, Rev. -

Certifiable Data Package (DAL A)

General Description

The Tri-Mode Ethernet MAC (TEMAC) DO-254 Certifiable Data Package is made up of the artifacts produced by applying the DO-254 lifecycle to the Xilinx® TEMAC IP and an encrypted version of the source code. This includes the following completed documents:

- Plan for Hardware Aspects of Certification
- Hardware Validation and Verification Plan
- Hardware Configuration Management Plan
- Hardware Design Plan
- Hardware Process Assurance Plan
- Hardware Validation and Verification Standard
- Hardware Requirements Standard
- Hardware Design Standard
- Hardware Requirements Document
- Hardware Design Document
- Hardware Configuration Index
- Verification Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
- Hardware Test Procedures
- Hardware Verification Results
- Hardware Elemental Analysis Results
- Hardware Requirements Traceability Matrix
- Hardware Accomplishment Summary

The above documents are available for certification efforts, however not all documents are included in the delivery package.

The TEMAC IP comprises the 10/100/1000 Mb/s, 1 Gb/s and 10/100 Mb/s Intellectual Property (IP) cores. This IP core is designed to support the AXI4 interface and is intended for Xilinx® Field Programmable Gate Arrays (FPGAs).

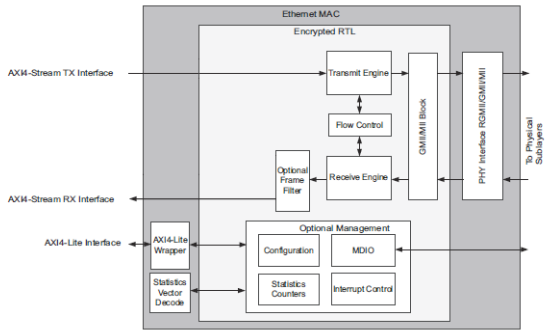
Safety Features

- Frame check sequence
- Frame type/length checking

Features

- Configurable half-duplex and full-duplex operation
- Supports 10/100 Mb/s, 1Gb/s, 2.5 Gb/s, or 10/100/1000 Mb/s IP cores
- Supports RGMII, GMII and MII as well as providing connectivity to
  - LogiCORE IP Ethernet 1000BASE-X PCS/PMA or SGMII using transceiver, SelectIO™ or Ten-Bit Interface (TBI)
- Optional MDIO interface to managed objects in PHY layers (MII Management)
- Optional frame filter with selectable number of table entries and optional statistics counters
- Supports Flow Control frames, Virtual LAN (VLAN) frames, jumbo frames and allows a configurable interframe gap

Block Diagram



Supported FPGA Families

Xilinx® 7-Series and Ultrascale™

Development Tools

ModelSim® v10.4 or later
Xilinx® Vivado® 2016.1 or later

Configuration

The DO-254 TEMAC IP is configurable as shown below:

Parameter Name	Allowable Values
C_FAMILY	aartix7, artix7, artix7l, artixu, azynq, kintex7, kintex7l, kintexu, qartix7, qkintex7, qkintex7l, qvirtex7, qzynq, virtex7, virtexu, zynq
C_INTERFACE	MII, GMII, RGMII, INTERNAL
C_MAC_SPEED	TRI_SPEED, SPEED_1000_MBPS, SPEED_10_100_MBPS
C_MDIO	0,1,2
C_HALF_DUPLEX	0,1
C_HAS_MMCM	0,1
C_HAS_BUFIO	0,1
C_HAS_HOST	0,1
C_ADD_FILTER	0,1
C_AT_ENTRIES	0-16
C_HAS_STATS	0,1
C_CNTR_RST	0,1
C_STATS_WIDTH	32, 64
C_PFC	0,1
C_INCLUDE_SHARE	0,1

Assumptions

Assumption 1: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system/safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.

Assumption 2: The objectives, activities and lifecycle data related specifically to the DO-254 TEMAC IP Core will be provided to the Integrator for inclusion into their overall certification package.

Assumption 3: Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

Assumption 4: All objectives related to the building, integration and Production (including Production Testing - ATP) of the system/LRU will be the responsibility of the integrator.

Assumption 5: Objectives related to hardware components other than the DO-254 TEMAC IP Core are the responsibility of the integrator.

Assumption 6: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 TEMAC IP Core in their system.

Assumption 7: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 TEMAC IP Core.

Assumption 8: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 TEMAC IP Core into their system.

Assumption 9: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System/Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 TEMAC IP Core at the system level.

Assumption 10: The integrator is required to include a clock timing constraint for this DO-254 TEMAC IP Core. This clock timing constraint will define the clock rate at which the IP core will operate. It is recommended that the integrator defines this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An example UCF file will be provided in Chapter 3 of the 10132-UG, but it is for reference only.

Assumption 11: The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results indicate that all configurations required to attain 100% coverage are tested.

Assumption 12: Some testing of the DO-254 TEMAC IP Core was done on a test board, the integrator is responsible for complete IP black box testing in his system. ***In order to accomplish this black box testing, the integrator is recommended to design his PCB to have access to at least XX (number defined in 10132-UG) spare FPGA pins that can be connected to a logic analyzer.*** If the integrator chooses to do post place and route simulation on their system as an additional validation, Logicircuit will provide the necessary files for the DO-254 TEMAC IP Core.

Revision History

Revision	Reason/Description	Date	Subversion repository revision
-	Draft 5 has been formally released as Rev. -	12/6/2016	104