

## General Description

The Soft Error Mitigation DO-254 Certifiable Data Package is made up of the artifacts produced by applying the DO-254 lifecycle to the Xilinx® Soft Error Mitigation IP v3.4 and an encrypted version of the source code. This includes the following completed documents:

- Plan for Hardware Aspects of Certification
- Hardware Validation and Verification Plan
- Hardware Configuration Management Plan
- Hardware Design Plan
- Hardware Process Assurance Plan
- Hardware Validation and Verification Standard
- Hardware Requirements Standard
- Hardware Design Standard
- Hardware Requirements Document
- Hardware Design Document
- Hardware Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
- Verification Configuration Index
- Hardware Test Procedures
- Hardware Verification Results
- Hardware Elemental Analysis Results
- Hardware Requirements Traceability Matrix
- Hardware Accomplishment Summary

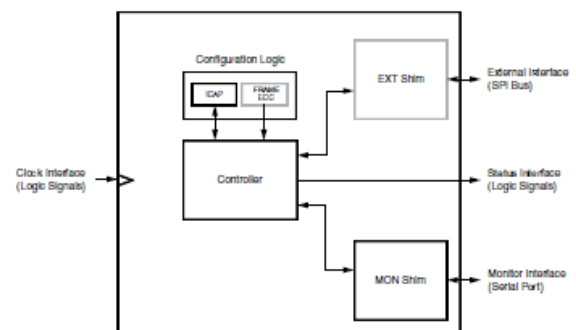
The above documents are available for certification efforts, however not all documents are included in the delivery package.

The DO-254 Soft Error Mitigation IP Core 1.00a, created and designed by Logicircuit, detects and corrects soft errors in Configuration Memory of Xilinx® FPGAs.

## Features

- Integration of built-in silicon primitives to fully leverage and improve upon the inherent error detection capability of the FPGA.
- Optional error correction using selectable method: repair, enhanced repair, or replace
  - Correction by repair method is ECC algorithm based.
  - Correction by enhanced repair method is ECC and CRC algorithm based.
  - Correction by replace method is data re-load based.
- Uses Xilinx® Essential Bits technology optional error classification to determine if a soft error has affected the function of the user design.
  - Increases uptime by avoiding disruptive recovery approaches for errors that have no real effect on design operation
  - Reduces effective failures-in-time (FIT).

## Block Diagram



## Supported FPGA Families

Xilinx® 7 Series and Spartan®-6

## Development Tools

Xilinx® EDK® 14.4 or later

ModelSim® v10.1c or later

Xilinx® ISIM 14.4 or later

Xilinx® XST 14.4 or later

Xilinx® Vivado® 2016.1 or later

## Configuration

The DO-254 Soft Error Mitigation Controller 1.00a is configurable as shown below:

Settable Parameter	Definition
C_FEATURE_SET	Defines the feature set.
C_DEVICE_ARRAY	Defines the device type
C_SCAN_START_ADDR	Indicates the starting LFA for read back (only applicable to Spartan®-6 devices)
C_SCAN_END_ADDR	Indicates the ending LFA for read back (only applicable to Spartan®-6 devices)
C_USEBIGADDR	Indicates if the external SPI Flash must use 32-bit addresses when set to '1', or 24-bit addresses when set to '0'
V_ENABLETIME	Indicates the bit rate for the monitor interface.

Settable Parameter	Definition
B_DEBUG	Enables the debug feature, and must always be set to 0 for implementation.
B_COSIM	Enables the hardware cosim feature, and must always be set to 0 for implementation.
B_DFSET	Defines if the monitor port is allowed to reset the controller with a new feature set, and must always be set to 0 for implementation.

## Assumptions

**Assumption 1:** The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system/safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.

**Assumption 2:** The objectives, activities and lifecycle data related specifically to the DO-254 Soft Error Mitigation Controller Core will be provided to the Integrator for inclusion into their overall certification package.

**Assumption 3:** Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation

decisions will be the responsibility of the integrator.

**Assumption 4:** All objectives related to the building, integration and production (including Production Testing — ATP) of the system/LRU will be the responsibility of the integrator.

**Assumption 5:** Objectives related to hardware components other than the DO-254 Soft Error Mitigation Controller Core are the responsibility of the integrator.

**Assumption 6:** The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-Soft Error Mitigation Controller Core in their system.

**Assumption 7:** The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 Soft Error Mitigation Controller Core.

**Assumption 8:** The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 Soft Error Mitigation Controller Core into their system.

**Assumption 9:** Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System/Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 Soft

Error Mitigation Controller Core at the system level.

**Assumption 10:** The integrator is required to include a clock timing constraint for this DO-254 Soft Error Mitigation Controller Core. This clock timing constraint will define the clock rate at which the IP core will operate. It is recommended that the integrator defines this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An example UCF file will be provided in Chapter 3 of the 10127-UG, but it is for reference only.

**Assumption 11:** The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results indicate that all configurations required to attain 100% coverage are tested.

**Assumption 12:** Some testing of the DO-254 Soft Error Mitigation Controller Core was done on a test board, the integrator is responsible for complete IP black box testing in their system to verify that the IP performs its intended function in the system. In order to assist the integrator with determining what should be tested at the system level, LogicCircuit has included a list of potential target tests in the “Potential Target Test” section of the User Guide for each IP. The integrator should evaluate the list of tests against the hardware functions of the IP they are using in their system to determine which tests they should perform at the system level.

### Revision History

Revision	Reason/Description	Date	Subversion repository revision
-	Draft 3 has been formally released as Rev. -	12/2/2013	115
A	PR-50-1664	2/15/2017	157
B	PR-50-1671	3/31/2017	169