LOGICIRCUIT

MicroBlaze

DO-254 Floating Point Operator v1.10a

8/9/2018, Rev. A

Certifiable Data Package (DAL A)

General Description

The Floating Point Operator DO-254 Certifiable Data Package is made up of the artifacts produced by applying the DO-254 lifecycle to the Xilinx® Floating Point Operator IP and an encrypted version of the source code. This includes the following completed documents:

- Plan for Hardware Aspects of Certification
- Hardware Validation and Verification Plan
- Hardware Configuration Management Plan
- Hardware Design Plan
- Hardware Process Assurance Plan
- Hardware Validation and Verification Standard
- Hardware Requirements Standard
- Hardware Design Standard
- Hardware Requirements Document
- Hardware Design Document
- Hardware Configuration Index
- Verification Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
- Hardware Test Procedures
- Hardware Verification Results
- Hardware Elemental Analysis Results
- Hardware Requirements Traceability Matrix
- Hardware Accomplishment Summary

The above documents are available for certification efforts, however not all documents are included in the delivery package.

The Floating Point IP provides the user with the means to perform floating point arithmetic on Xilinx® Field Programmable Gate Arrays (FPGAs).

Features

- Supports the following operators:
  - Multiply
  - Divide
  - Add
  - Square Root
  - Conversion from floating-point to fixed-point
  - Conversion from fixed-point to floating-point
  - Comparison (greater than and less than)
- Compliance with IEEE-754 Standard
- Parameterized fraction and exponent wordlengths for most operators
- Optimized for speed
- Fully synchronous design using a single clock

Supported FPGA Families

Xilinx® Kintex®-7, Virtex®-7, Artix®-7, Zynq®, Zynq®UltraScale+™, Artix® UltraScale™, Virtex® UltraScale™, Kintex® UltraScale™

Development Tools

ModelSim® v10.4 or later
Xilinx® Vivado® 2016.1 or later

Configuration

The DO-254 Floating Point IP is configurable as shown below:

Settable Parameter	Allowable Values
C_XDEVICEFAMILY	"kintex7", "virtex7", "artix7", "zynq", "zynquplus", "artixu", "virtexu", "kintexu"

Settable Parameter	Allowable Values
C_HAS_ADD	0, 1
C_HAS_MULTIPLY	0, 1
C_HAS_DIVIDE	0, 1
C_HAS_COMPARE	0, 1
C_HAS_FIX_TO_FLT	0, 1
C_HAS_FLT_TO_FIX	0, 1
C_HAS_SQRT	0, 1
C_A_WIDTH	23, 32, 48, 64
C_A_FRACTION_WIDTH	0,16, 24, 40, 53
C_B_WIDTH	32, 48, 64
C_B_FRACTION_WIDTH	24, 40, 53
C_RESULT_WIDTH	1, 16, 32, 48, 64
C_RESULT_FRACTION_ WIDTH	0, 24, 40, 53
C_COMPARE_ OPERATION	1, 4
C_LATENCY	0-28
C_MULT_USAGE	0, 2
C_HAS_DIVIDE_BY_ZERO	0, 1
C_HAS_B	0, 1
C_HAS_RESULT_TUSER	0, 1
C_A_TDATA_WIDTH	24, 32, 48, 64
C_B_TDATA_WIDTH	32, 48, 64
C_RESULT_TDATA_ WIDTH	8, 16, 32, 48, 64
C_THROTTLE_SCHEME	1, 2, 3, 4

Settable Parameter	Allowable Values
C_HAS_ACLKEN	0, 1
C_HAS_ARESETN	0, 1
C_HAS_UNDERFLOW	0, 1
C_HAS_OVERFLOW	0, 1
C_RESULT_TUSER_WIDTH	1-3
C_OPTIMIZATION	0, 1
C_HAS_OPERATION	0, 1

Assumptions

Assumption 1: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system / safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.

Assumption 2: The objectives, activities and lifecycle data related specifically to the DO-254 Floating Point IP Core will be provided to the Integrator for inclusion into their overall certification package.

Assumption 3: Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

Assumption 4: All objectives related to the building, integration and Production (including Production Testing - ATP) of the system/LRU will be the responsibility of the integrator.

Assumption 5: Objectives related to hardware components other than the DO-254 Floating Point IP Core are the responsibility of the integrator.

Assumption 6: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 Floating Point IP Core in their system.

Assumption 7: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 Floating Point IP Core.

Assumption 8: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 Floating Point IP Core into their system.

Assumption 9: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System / Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 Floating Point IP Core at the system level.

Assumption 10: The integrator is required to include a clock timing constraint for this DO-254 Floating Point IP Core. This clock timing constraint will define the clock rate at which the IP core will operate. It is recommended that the integrator defines this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An example UCF file will be provided in Chapter 3 of the 10128-UG, but it is for reference only.

Assumption 11: The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results indicate that all configurations required to attain 100% coverage are tested.

Assumption 12: Some testing of the DO-254 Floating Point IP Core was done on a test board, the integrator is responsible for complete IP black box testing in their system to verify that the IP performs its intended function in the system. In order to assist the integrator with determining what should be tested at the system level, Logicircuit has included a list of potential target tests in the “Potential Target Test” section of the User Guide for each IP. The integrator should evaluate the list of tests against the hardware functions of the IP they are using in their system to determine which tests they should perform at the system level.

Revision History

Revision	Reason/Description	Date	Subversion repository revision
-	Draft 2 has been formally released as Rev. -	10/6/2016	102
A	PR-1-17	8/9/2018	178