



**Questions?**  
 Don't see what you need?  
 Reach out to us at:  
 770.887.7293  
 info@logiccircuit.com

DO-254 SafeIP™	Xilinx V	U	U+	X7	S6	Vivado Version	ISE Version
<b>Microprocessors</b>							
MicroBlaze® 1.00a	v8.20			X7	S6		13.4 or later
<b>SEM</b>							
UltraScale Soft Error Mitigation Controller 1.00a	v3.1	U				2016.4 or later	
UltraScale+ Soft Error Mitigation Controller 1.00a	v3.1		U+			2019.1 or later	
Soft Error Mitigation 1.01a	v3.4			X7	S6	2016.1 or later	14.4 or later
<b>Avionics</b>							
AFDX (ARINC 664 Part 7) 1.00a	v2.8	U		X7		2016.1 or later	14.4 or later
ARINC 818 XGA Transceiver Core 1.00a					S6		14.5 or later
ARINC 429 Transceiver Receiver Core 1.00a				X7	S6	2016.1 or later	14.4
MIL-STD-1553 1.00a						Microsemi IGLOO2 Family	Libero Version 11.9.0.4
<b>AXI</b>							
AXI-4 Lite IP Interface (IPIF) 1.01a	v1.01.a	U		X7	S6	2015.3 or later	14.4 or later
AXI General Purpose Input/Output (GPIO) 1.00a	v1.01.b			X7	S6		13.4 or later
AXI Interconnect 1.10a	v1.06.a		U+	X7		2016.1 or later	14.6 or later
AXI Serial Peripheral Interface (SPI) 1.00a	v1.02.a			X7	S6		14.3 or later
AXI Universal Asynchronous Receiver Transmitter (UART) 16550 1.00a	v1.01.a			X7	S6		13.4 or later
AXI Interrupt Controller 1.00a	v1.01.a			X7	S6		13.4 or later
AXI Timer 1.00a	v1.03.a			X7	S6		14.5 or later
AXI Timebase Watchdog Timer 1.00a				X7	S6		13.4 or later

<b>DO-254 SafeIP™</b>	<b>Xilinx V</b>	<b>U</b>	<b>U+</b>	<b>X7</b>	<b>S6</b>	<b>Vivado Version</b>	<b>ISE Version</b>
<b>AXI 7-Series DDRx (Limited) 1.01a</b>	v1.8			<b>X7</b>		2017.4 or later	14.4 or later
<b>AXI Memory Mapped to PCI Express (PCIe) 1.00a</b>	v2.8			<b>X7</b>		2019.1 or later	
<b>AXI to PCI Bridge 1.00a</b>	v3 v4			<b>X7</b>	<b>S6</b>		13.3 or later
<b>Memory Functions</b>							
<b>7-Series DDRx (Native Limited) 1.00a</b>	v1.8			<b>X7</b>		2019.1 or later	14.4 or later
<b>External Memory Controller 1.00a</b>	v1.03.a			<b>X7</b>	<b>S6</b>		14.5 or later
<b>Local Memory Bus (LMB) 1.00a</b>	v2.00.b			<b>X7</b>	<b>S6</b>		14.6
<b>LMB BRAM Interface Controller 1.00a</b>	v3.00.b			<b>X7</b>	<b>S6</b>		14.6
<b>Processor System Reset Module 1.02a</b>	v3.00.a			<b>X7</b>	<b>S6</b>	2016.1 or later	14.4 or later
<b>Block Memory Generator 1.00a</b>	v8.0			<b>X7</b>	<b>S6</b>		14.4 or later
<b>Distributed Memory Generator 1.00a</b>	v8.0			<b>X7</b>	<b>S6</b>		14.4 or later
<b>FIFO Generator 1.00a</b>	v10.0			<b>X7</b>	<b>S6</b>		14.4 or later
<b>Interfaces</b>							
<b>Tri-Mode Ethernet MAC (TEMAC) 1.00a</b>	v9.0	<b>U</b>		<b>X7</b>		2016.1 or later	
<b>Math Functions</b>							
<b>Floating Point Operator 1.10a (limited configuration)</b>	v7.0	<b>U</b>		<b>X7</b>		2016.1 or later	
<b>Bridges</b>							
<b>Integrated Block for PCIe 1.10a</b>			<b>U+</b>	<b>X7</b>		2016.1 or later	
<b>ZIPCores</b>							
	<b>ZIPC V</b>						
<b>I2C Master Serial Interface Controller 1.11a</b>	v1.1			<b>X7</b>	<b>S6</b>	2016.1 or later	14.4 or later
<b>Multi-Format Video Deinterlacer 1.00a</b>	v1.2			<b>X7</b>	<b>S6</b>	2016.1 or later	14.4 or later
<b>UART Serial Interface Controller 1.00a</b>	v1.0			<b>X7</b>	<b>S6</b>	2016.1 or later	14.4 or later
<b>Digital Video Scaler 1.00a</b>	v2.1			<b>X7</b>	<b>S6</b>	2016.1 or later	14.6 or later

