DO-254 Avionics Full-Duplex Switched Ethernet (AFDX) 1.00a Certifiable Data Package (DAL A)

04/08/2015, Preliminary Revision

General Description

Avionics Full-Duplex Switched Ethernet (AFDX) Endpoint IP Core for Xilinx 7 Series FPGA and Zynq SoC families, inclusive of DO-254 Certifiable Data Package. The AFDX Endpoint IP is fully compliant to ARINC 664 Part 7 with a DO-254 DAL A Certifiable Data Package including artifacts produced by a fully compliant lifecycle.

IP Core Features

The AFDX core is implemented in hardware with an AXI interface for control processor such as MicroBlaze, Zynq PS, or other external processor.

Built-in safety features common to AFDX:

- Redundancy Management
- Integrity Checker
- Deterministic Packet Delivery

Supported AFDX capabilities:

- Fully compliant dual-channel ARINC 664 Part 7 IP
- Integrated redundancy manager
- IEEE 802.3 10/100/1000 Mbps Full-Duplex links
- IP/UDP layers handled internally
- Up to 128 Output VL's and up to 512 Input VL's
- Up to 1024 Output Ports
- Up to 4096 Sampling or Queuing Input Ports
- Selectable Internal (within the IP)/External MAC
- Selectable MII, GMII, or RGMII interface
- AXI4-Lite Interface for setting registers
- Optional AXI4 master for Rx and Tx DMA operations

The AFDX core is highly configurable to meet the needs of various avionics systems or other platforms. See the configuration section of this document.

Certifiable Process and Documentation

Logicircuit applies a standard process to all of its IP cores and conducts all activities associated with a DO-254 DAL A process, including generation of full documentation and review artifacts.

Certification Documentation Generated:

- Plan for Hardware Aspects of Certification
- Hardware Validation and Verification Plan
- Hardware Configuration Management Plan
- Hardware Design Plan
- Hardware Process Assurance Plan
- Hardware Validation and Verification Standard
- Hardware Requirements Standard
- Hardware Design Standard
- Hardware Requirements Document
- Hardware Design Document
- Hardware Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
- Verification Configuration Index
- Hardware Test Procedures
- Hardware Verification Results
- Hardware Elemental Analysis Results
- Hardware Requirements Traceability Matrix
- Hardware Accomplishment Summary

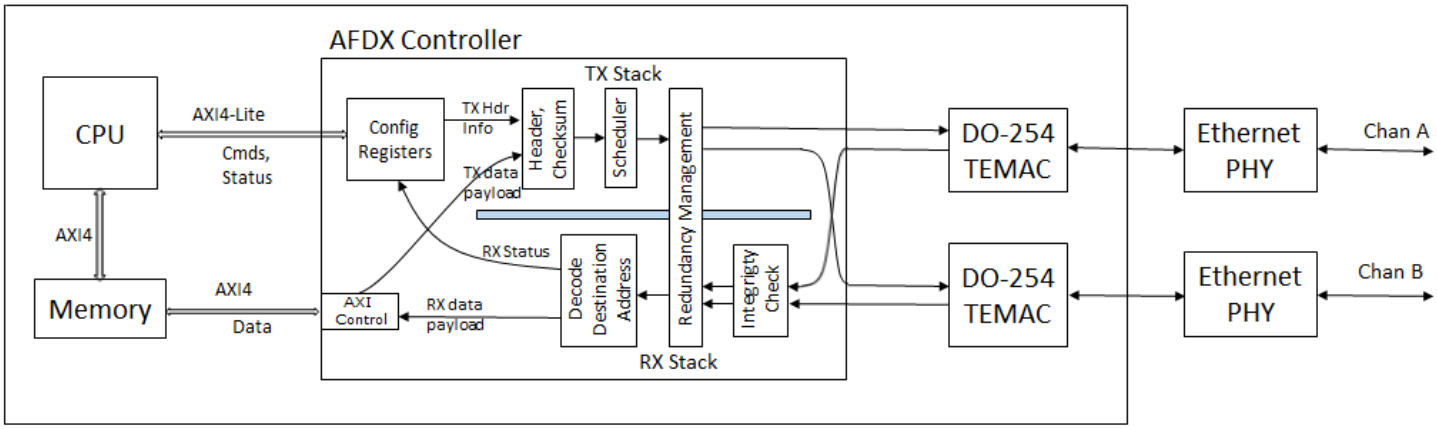
A subset of the artifacts is delivered as part of standard IP delivery, and all artifacts are available for audit.

Supported Device Families

Xilinx® 7-Series FPGAs and Zynq-7000 SOCs
UltraScale and other families on request

Development Tools

Xilinx® ISE/EDK® 14.6 or later
Vivado 2014.4 and later
ModelSim® v10.2c or later
Xilinx® ISIM 14.6 or later
Xilinx® XST 14.6 or later



Core Configuration

The DO-254 AFDX version 1.00a is configurable as shown below:

Settable Parameter	Definition
C_FAMILY	Specifies the FPGA family being used
C_BASEADDR	Specifies the 32-bit AXI Base Address
C_HIGHADDR	Specifies the 32-bit AXI High Address
C_S_AXI_ADDR_WIDTH	Specifies the AXI address bus width
C_S_AXI_DATA_WIDTH	Specifies the AXI data bus width
C_SPEED	Specifies 10/100/1000 data rate
C_NUM_VLINKS	Specifies number of Virtual Links
C_BAG	Specifies minimum time between packets
C_L_MAX	Specifies maximum Ethernet frame length
C_USE_DMA	Specifies whether an internal DMA is used to read/write data
C_USE_QUEING	Specifies whether Rx ports use Queing. Default is Sampling.
C_USE_EXTERNAL_MAC	Specifies whether external MAC is used. Default is internal.
C_ENET_INTERFACE	Specifies MII, GMII, or RGMII

DO-254 AFDX Integration Requirements

1: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system/safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.

2: The objectives, activities and lifecycle data related specifically to the DO-254 AFDX Core will be provided to the Integrator with guidance for inclusion into their overall certification package.

3: Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

4: All objectives related to the building, integration and production (including Production Testing — ATP) of the system/LRU will be the responsibility of the integrator.

5: Objectives related to hardware components other than the DO-254 AFDX Core are the responsibility of the integrator.

6: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 AFDX Core in their system.

7: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 AFDX Core.

8: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 AFDX Core into their system.

9: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System/Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 AFDX Core at the system level.

10: The integrator is required to include a clock timing constraint for this DO-254 AFDX Core. This clock timing constraint will define the clock rate at which the IP core will operate. It is recommended that the integrator defines this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An example UCF file will be provided in Chapter 3 of the 10130-UG, but it is for reference only.

11: The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results indicate that all configurations required to attain 100% coverage are tested.

12: Some testing of the DO-254 AFDX Core was done on a test board, the integrator is responsible for complete IP black box testing in his system. In order to accomplish black box testing, the integrator is recommended to design the PCB to have access to at least XX (number defined in 10130-UG) spare FPGA pins that can be connected to a logic analyzer.

13. If the integrator chooses to do post place and route simulation on their system as an additional validation, Logicircuit will provide the necessary files for the DO-254 AFDX Core.