LOGICIRCUIT

MicroBlaze

DO-254 Fast Simplex Link 1.00a Certifiable Data Package (DAL A)

November 28, 2012, Revision -

General Description

The Fast Simplex Link (FSL) DO-254 Certifiable Data Package is made up of the artifacts produced by applying the DO-254 lifecycle to the Xilinx® FSL IP v2.11e and an encrypted version of the source code. This includes the following completed documents:

- Plan for Hardware Aspects of Certification
- Hardware Validation and Verification Plan
- Hardware Configuration Management Plan
- Hardware Design Plan
- Hardware Process Assurance Plan
- Hardware Validation and Verification Standard
- Hardware Requirements Standard
- Hardware Design Standard
- Hardware Requirements Document
- Hardware Design Document
- Hardware Elemental Analysis Results
- Hardware Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
- Hardware Test Procedures
- Hardware Verification Results
- Hardware Elemental Analysis Results
- Hardware Requirements Traceability Matrix
- Hardware Accomplishment Summary

The above documents are available for certification efforts, however not all documents are included in the delivery package.

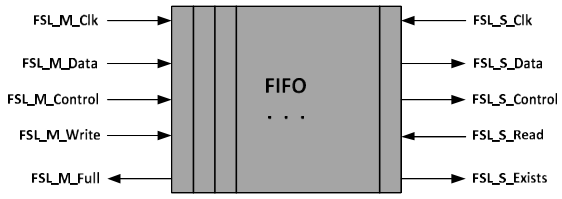
The DO-254 Fast Simplex Link (FSL) IP Core 1.00a, created and designed by Logicircuit, is an uni-directional point-to-point communication channel bus used to perform fast communication. The FSL IP interfaces are used to transfer data to and from the register file on the processor hardware on the Field Programmable Gate Arrays (FPGAs).

This version of the DO-254 FSL IP 1.00a does not have any built-in safety features

Features

- Implements a uni-directional point to point FIFO based communication
- Provides a mechanism for unshared and non-arbitrated communication. This can be used for fast transfer of data words between a master and a slave, thus implementing the FSL interface.
- Provides an extra control bit for annotating transmit data. This bit can be used by the slave-side interface for different purposes, such as decoding the transmit word as a control word, or using the bit to indicate the start or end of frame transmission.
- FIFO depths can be as low as 1K and as high as 8K.
- Supports synchronous and asynchronous FIFO modes. This allows the master and slave side of the FSL to clock at different rates.
- Support for SRL16 and dual port LUT RAM or block RAM based FIFO implementation.

Block Diagram



Supported FPGA Families

Xilinx® 7-Series and Spartan®-6

Development Tools

Xilinx® ISE/EDK® 13.4 or later
ModelSim® v10.1b or later (models required)
Xilinx® ISIM 13.4 or later (no models required)
Xilinx® XST 13.4 or later
Precision Synthesis 2012b or later

Configuration

The DO-254 FSL version 1.00a is configurable as shown below:

Category	Settable Parameter
Clocking Modes	C_ASYNC_CLKS
Use BRAMs for FIFO	C_IMPL_STYLE
FSL Bus Width	C_FSL_DWIDTH
FSL FIFO Depth C_ASYNC_CLKS=0 C_ASYNC_CLKS=1 and C_IMP_STYLE=0 C_ASYNC_CLKS=1 and C_IMP_STYLE=1	C_FSL_DEPTH
Propagate Control Bit	C_USE_CONTROL
Level of external reset	C_EXT_RESET_HIGH
Period of FSL_S_CLK in ps.	C_READ_CLOCK_PERIOD

Assumptions

Assumption 1: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system/safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.
The objectives, activities and lifecycle data related specifically to the DO-254 FSL IP Core 1.00a will be provided to the Integrator for inclusion into their overall certification package.
Assumption 2: Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

Assumption 3: Logicircuit will coordinate with the Certification Authority related only to DO-254 compliance with the DO-254 FSL IP Core 1.00a.

Assumption 4: All objectives related to the building, integration and Production (including Production Testing - ATP) of the system/LRU will be the responsibility of the integrator.

Assumption 5: Objectives related to hardware components other than the DO-254 FSL IP Core 1.00a are the responsibility of the integrator.

Assumption 6: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 FSL IP Core 1.00a in their system.

Assumption 7: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 FSL IP Core 1.00a.

Assumption 8: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 FSL IP Core 1.00a into their system.

Assumption 9: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System/Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 FSL IP Core 1.00a at the system level.

Assumption 10: The integrator is required to include a clock timing constraint for this DO-254 FSL IP Core 1.00a. This clock timing constraint will define the clock rate at which the IP core will operate. It is recommended that the integrator define this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An example UCF file will be provided in 10102-UG, but it is for reference only.

Assumption 11: The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results will indicate that all configurations required to attain 100% coverage are tested.

Simulation validation for the DO-254 FSL IP Core 1.00a is being done on a test board. The integrator must revalidate a portion of this simulation on the integrator's target. Logicircuit will provide the files and data necessary to perform this revalidation in 10102-UG.

In order to accomplish this revalidation, the integrator is required to design his PCB to have access to at least 21 spare FPGA pins that can be connected to a logic analyzer.

If the integrator chooses to do post place and route simulation on their system as an additional validation (again, this would only be a portion of Logicircuit's simulation), Logicircuit will provide the necessary files for the DO-254 FSL IP Core 1.00a.