General Description

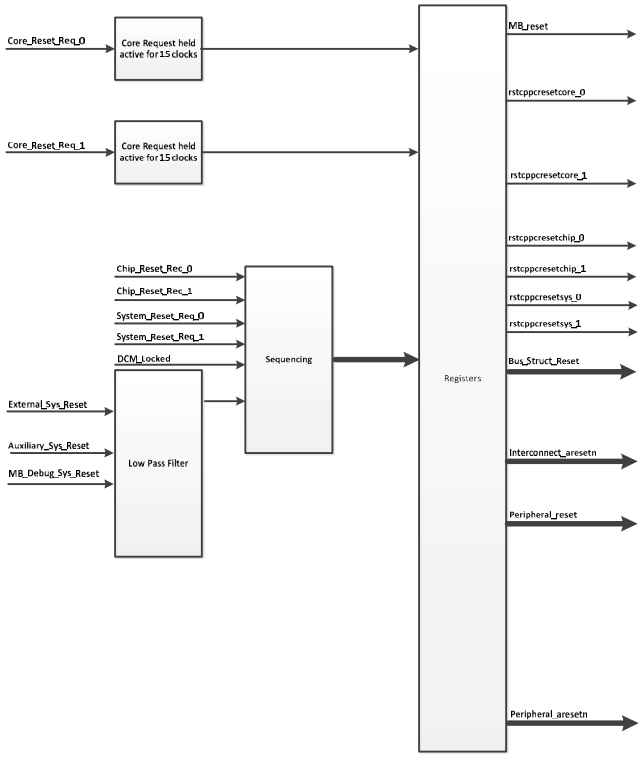
The Processor System Reset DO-254 Certifiable Data Package is made up of the artifacts produced by applying the DO-254 lifecycle to the Xilinx® Processor System Reset IP and an encrypted version of the source code. This includes the following completed documents:

- Plan for Hardware Aspects of Certification
- Hardware Validation and Verification Plan
- Hardware Configuration Management Plan
- Hardware Design Plan
- Hardware Process Assurance Plan
- Hardware Validation and Verification Standard
- Hardware Requirements Standard
- Hardware Design Standard
- Hardware Requirements Document
- Hardware Design Document
- Hardware Elemental Analysis Results
- Hardware Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
- Hardware Test Procedures
- Hardware Verification Results
- Hardware Elemental Analysis Results
- Hardware Requirements Traceability Matrix
- Hardware Accomplishment Summary

The above documents are available for certification efforts, however not all documents are included in the delivery package.

The Processor System Reset core provides a reset function allowing users to customize their designs to suit their application by setting certain parameters to enable/disable features.

Block Diagram



Features

- Asynchronous external reset input is synchronized with clock
- Asynchronous auxiliary external reset input is synchronized with clock
- Both the external and auxiliary reset inputs are selectable active high or active low
- Selectable minimum pulse width for reset inputs to be recognized
- Selectable load equalizing
- DCM Locked input
- Power On Reset generation
- Parametized Active Low Reset signal generation for core and for interconnect

Features (cont)

- Sequencing of reset signals coming out of reset:
  - First: Bus structures come out of reset (Interconnect, AXI and bridges, for example)
  - Second: Peripheral(s) come out of reset 16 clocks later (UART, SPI, IIC for example)
  - Third: The CPU(s) comes out of reset 16 clocks after the peripherals

Supported FPGA Families

Xilinx® 7-Series and Spartan®-6

Development Tools

Xilinx® ISE/EDK® 13.4 or later
ModelSim® v10.1b or later (models required)
Xilinx® ISIM 13.4 or later (no models required)
Xilinx® XST 13.4 or later
Precision Synthesis 2012b or later

Configuration

The DO-254 LMB version 1.00a is configurable as shown below:

Settable Parameter	***Label in GUI***
C_EXT_RST_WIDTH	Number of Clocks Before Input Change is Recognized On The External Reset Input
C_AUX_RST_WIDTH	Number of Clocks Before Input Change is Recognized On The Auxiliary Reset Input
C_EXT_RESET_HIGH	External Reset Active High
C_AUX_RESET_HIGH	Auxiliary Reset Active High
C_NUM_BUS_RST	Number of Bus Structure Reset Registered Outputs
C_NUM_PERP_RST	Number of Peripheral Reset Registered Outputs
C_NUM_INTERCONNECT_ARESETN	Number of Active Low Interconnect Reset Registered Outputs
C_NUM_PERP_ARESETN	Number of Active Low Peripheral Reset Registered Outputs

Assumptions

Assumption 1: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system / safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.
The objectives, activities and lifecycle data related specifically to the DO-254 Processor System Reset IP Core will be provided to the Integrator for inclusion into their overall certification package.

Assumption 2: Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

Assumption 3: Logicircuit will coordinate with the Certification Authority related only to DO-254 compliance with the DO-254 Processor System Reset IP Core.

Assumption 4: All objectives related to the building, integration and Production (including Production Testing - ATP) of the system/LRU will be the responsibility of the integrator.

Assumption 5: Objectives related to hardware components other than the DO-254 Processor System Reset IP Core are the responsibility of the integrator.

Assumption 6: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 Processor System Reset IP Core in their system.

Assumption 7: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 Processor System Reset IP Core.

Assumption 8: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 Processor System Reset IP Core into their system.

Assumption 9: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System / Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 Processor System Reset IP Core at the system level.

Assumption 10: The integrator is required to include a clock timing constraint for this DO-254 Processor System Reset IP core. This clock timing constraint will define the clock rate at which the IP core will operate. It is recommended that the integrator define this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An example UCF file will be provided in 10108-UG, but it is for reference only.

Assumption 11: The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results will indicate that all configurations required to attain 100% coverage are tested.

Simulation validation for the DO-254 Processor System Reset 1.00 is being done on a test board. The integrator must revalidate a portion of this simulation on the integrator's target. Logicircuit will provide the files and data necessary to perform this revalidation in 10108-UG.

In order to accomplish this revalidation, the integrator is required to design his PCB to have access to at least 13 spare FPGA pins that can be connected to a logic analyzer.

If the integrator chooses to do post place and route simulation on their system as an additional validation (again, this would only be a portion of Logicircuit's simulation), Logicircuit will provide the necessary files for the DO-254 Processor System Reset IP.