General Description

The MicroBlaze® DO-254 Certifiable Data Package is made up of the artifacts produced by applying the DO-254 lifecycle to the Xilinx™ MicroBlaze® IP and an encrypted version of the source code. This includes the following completed documents:

- Plan for Hardware Aspects of Certification
- Hardware Validation and Verification Plan
- Hardware Configuration Management Plan
- Hardware Design Plan
- Hardware Process Assurance Plan
- Hardware Validation and Verification Standard
- Hardware Requirements Standard
- Hardware Design Standard
- Hardware Requirements Document
- Hardware Design Document
- Hardware Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
- Verification Configuration Index
- Hardware Test Procedures
- Hardware Verification Results
- Hardware Elemental Analysis Results
- Hardware Requirements Traceability Matrix
- Hardware Accomplishment Summary

The above documents are available for certification efforts, however not all documents are included in the delivery package.

The DO-254 MicroBlaze® IP Core created and designed by Xilinx™, is a 32-bit reduced instruction set computer (RISC) embedded soft core processor optimized for implementation in Xilinx™ Field Programmable Gate Arrays (FPGAs).

Safety Features

This version of the Xilinx® MicroBlaze® IP has the following safety features:

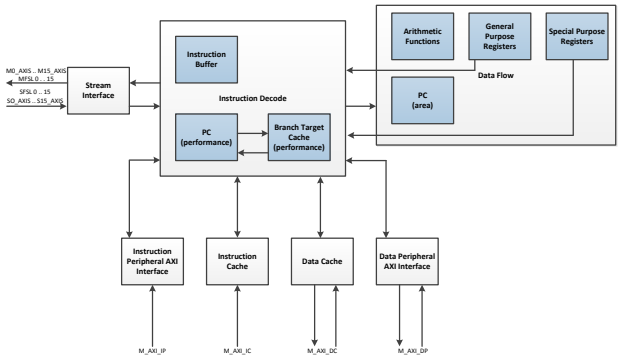
- Error Detection and Correction
  - LMB BRAM Memory
- Parity protection
  - Internal BRAMs and Caches
- OpCode Monitoring and Exceptions
  - Instruction Bus Exception
  - Illegal OpCode Exception
  - Stack Protection Violation Exception
  - Unaligned Access Exception
  - Data Bus Exception
  - Divide Exception
  - Floating Point Exception
  - Stream Exception
- Lockstep
- Optional exclusion of SRLs and LUTRAM

Features

This version of the Xilinx® MicroBlaze® IP does not incorporate the following subset of features:

- MMU (Memory Management Unit)
- PLBv46 Bus
- Debug Module
- Hardware breaks
- XCL (CacheLink bus)
- AXI exclusive access

Block Diagram



Supported FPGA Families

Xilinx®-7 Series and Spartan®-6

Development Tools

Xilinx® ISE/EDK® 13.4 or later
ModelSim® v10.1c or later
Xilinx® ISIM 13.4 or later
Xilinx® XST 13.4 or later

Configuration

The DO-254 MicroBlaze® version 1.00a is configurable as shown below:

Settable Parameter	Label in EDK
C_AREA_OPTIMIZED	Select implementation to optimize area (with lower instruction throughput)
C_USE_BARREL	Enable Barrel Shifter
C_USE_FPU	Enable Floating Point Unit
C_USE_HW_MUL	Enable Integer Multiplier
C_USE_DIV	Enable Integer Divider
C_USE_MSR_INSTR	Enable Additional Machine Status Register Instructions
C_USE_PCMP_INSTR	Enable Pattern Comparator
C_USE_EXTENDED_FSL_INSTR	Enable Additional Stream Instructions
C_USE_BRANCH_TARGET_CACHE	Enable Branch Target Cache
C_BRANCH_TARGET_CACHE_SIZE	Branch Target Cache Size
C_FAULT_TOLERANT	Enable Fault Tolerance Support
C_FPU_EXCEPTION	Enable Floating Point Unit Exceptions
C_DIV_ZERO_EXCEPTION	Enable Integer Divide Exception
C_M_AXI_I_BUS_EXCEPTION	Enable Instruction-side AXI Exception
C_M_AXI_D_BUS_EXCEPTION	Enable Data-side AXI Exception
C_ILL_OPCODE_EXCEPTION	Enable Illegal Instruction Exception
C_OPCODE_0X0_ILLEGAL	Generate Illegal Instruction Exception for NULL Instruction
C_USE_STACK_PROTECTION	Enable stack protection
C_UNALIGNED_EXCEPTIONS	Enable Unaligned Data Exception
C_FSL_EXCEPTION	Enable Stream Exception
C_USE_ICACHE	Enable Instruction Cache
C_CACHE_BYTE_SIZE	Size in Bytes (Instruction Cache Feature)
C_ICACHE_LINE_LEN	Line Length (Instruction Cache Feature)
C_ICACHE_BASEADDR	Base Address (Instruction Cache Feature)
C_ICACHE_HIGHADDR	High Address (Instruction Cache Feature)
C_ALLOW_ICACHE_WR	Enable Writes (Instruction Cache Feature)

Settable Parameter	Label in EDK
C_ICACHE_ALWAYS_USED	Use Cache Links for All Memory Accesses (Instruction Cache Feature)
C_ICACHE_FORCE_TAG_LUTRAM	Use Distributed RAM for Tags (Instruction Cache Feature)
C_ICACHE_STREAMS	Number of Streams (Instruction Cache Feature)
C_ICACHE_VICTIMS	Number of Victims (Instruction Cache Feature)
C_ICACHE_DATA_WIDTH	Data Width (Instruction Cache Feature)
C_USE_DCACHE	Enable Data Cache
C_DCACHE_BYTE_SIZE	Size in Bytes (Data Cache Feature)
C_DCACHE_LINE_LEN	Line Length (Data Cache Feature)
C_DCACHE_BASZEADDR	Base Address (Data Cache Feature)
C_DCACHE_HIGHADDDR	High Address (Data Cache Feature)
C_ALLOW_DCACHE_WR	Enable Writes (Data Cache Feature)
C_DCACHE_ALWAYS_USED	Use Cache Links for All Memory Accesses (Data Cache Feature)
C_DCACHE_FORCE_TAG_LUTRAM	Use Distributed RAM for Tags (Data Cache Feature)
C_DCACHE_USE_WRITEBACK	Enable Write-back Storage Policy (Data Cache Feature)
C_DCACHE_VICTIMS	Number of Victims (Data Cache Feature)
C_DCACHE_DATA_WIDTH	Data Width (Data Cache Feature)
C_INTERRUPT_IS_EDGE	Sense Interrupt on Edge vs. Level
C_EDGE_IS_POSITIVE	Sense Interrupt on Rising vs. Falling Edge
C_RESET_MSR	Reset Value for Select MSR Bits
C_PVR	Specifies Processor Version Register
C_PVR_USER1	USER1 Bits in Processor Version Register
C_PVR_USER2	USER2 Bits in Processor Version Registers

Assumptions

Assumption 1: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system/safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.

Assumption 2: The objectives, activities and lifecycle data related specifically to the DO-254 MicroBlaze® IP Core will be provided to the Integrator for inclusion into their overall certification package.

Assumption 3: Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

Assumption 4: All objectives related to the building, integration and Production (including Production Testing - ATP) of the system/LRU will be the responsibility of the integrator.

Assumption 5: Objectives related to hardware components other than the DO-254 MicroBlaze® IP Core are the responsibility of the integrator.

Assumption 6: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 MicroBlaze® IP Core in their system.

Assumption 7: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 MicroBlaze® IP Core.

Assumption 8: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 MicroBlaze® IP Core into their system.

Assumption 9: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System/Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 MicroBlaze® IP Core at the system level.

Assumption 10: The integrator is required to include a clock timing constraint for this DO-254 MicroBlaze® IP Core. This clock timing constraint will define the clock rate at which the IP core will operate. It is recommended that the integrator define this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An example UCF file will be provided in 10100-UG, but it is for reference only.

Assumption 11: The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results will indicate that all configurations required to attain 100% coverage are tested.

Assumption 12: Simulation validation for the DO-254 MicroBlaze® IP Core is being done on a test board. The integrator is responsible for black box testing in his system. ***In order to accomplish this black box testing, the integrator is recommended to design his PCB to have access to at least XX (number defined in 10100-UG) spare FPGA pins that can be connected to a logic analyzer.*** If the integrator chooses to do post place and route simulation on their system as an additional validation, Logicircuit will provide the necessary files for the DO-254 MicroBlaze® IP Core.

Revision History

Revision	Reason/Description	Date	Subversion repository revision
-	Initial Release	9/2/2014	175