General Description

The AXI Interconnect DO-254 Certifiable Data Package is made up of the artifacts produced by applying the DO-254 lifecycle to the Xilinx® AXI Interconnect IP v1.06a and an encrypted version of the source code. This includes the following completed documents:

- Plan for Hardware Aspects of Certification
- Hardware Validation and Verification Plan
- Hardware Configuration Management Plan
- Hardware Design Plan
- Hardware Process Assurance Plan
- Hardware Validation and Verification Standard
- Hardware Requirements Standard
- Hardware Design Standard
- Hardware Requirements Document
- Hardware Design Document
- Hardware Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
- Verification Configuration Index
- Hardware Test Procedures
- Hardware Verification Results
- Hardware Elemental Analysis Results
- Hardware Requirements Traceability Matrix
- Hardware Accomplishment Summary

The above documents are available for certification efforts, however not all documents are included in the delivery package.

The DO-254 AXI Interconnect IP Core 1.00a, created and designed by Logicircuit, connects one or more AXI memory-mapped master devices to one or more memory-mapped slave devices in Xilinx Field Programmable Gate Arrays (FPGAs).

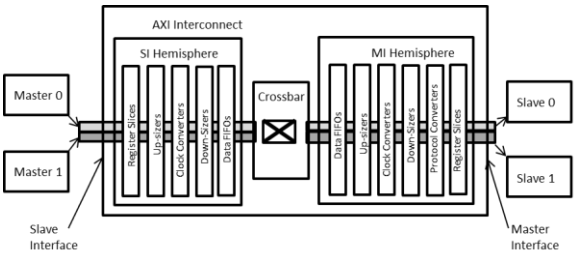
This version of the DO-254 AXI Interconnect IP 1.00a does not have any built-in safety features.

Features

- AXI protocol compliant (AXI4 only), including:
  - Burst lengths up to 256 for incremental (INCR) bursts
  - Propagates Quality of Service (QoS) signals, if any; not used by the AXI Interconnect core (optional)
- Interface data widths:
  - 32, 64, 128, 256, 512, or 1024 bits
- Address width: 12 to 64 bits
- Up to 16 Slave interfaces (to accept transactions from up to 16 connected master devices) and one Master Interface (to issue transactions to one connected slave device)
  - When connecting one master to one slave, the AXI Interconnect core can optionally perform any of the optional data-width conversions, clock-rate conversions, register pipelining, and datapath buffering functions
- Built-in data-width conversion:
  - Each master and slave connection can independently use data widths of 32, 64, 128, 256, 512, or 1024 bits:
    - The internal crossbar can be configured to have a native data width of 32, 64, 128, 256, 512, or 1024 bits.
    - Data-width conversion is performed for each master and slave connection that

does not match the crossbar native data width.
    - When converting to a wider interface (upsizing), data is packed (merged) when permitted by address channel control signals (CACHE modifiable bit is asserted).
    - When converting to a narrower interface (downsizing), burst transactions are split into multiple transactions if the maximum burst length otherwise would be exceeded.
- Built-in clock-rate conversion
- Optional register-slice pipelining
- Optional datapath FIFO buffering
- Supports multiple outstanding transactions
- Fixed priority and round-robin arbitration
- Support for Read-only and Write-only master devices, resulting in reduced resource utilization

Core Diagram



Supported FPGA Families

Xilinx® 7-Series

Development Tools

Xilinx® ISE/EDK® 14.6 or later
QuestaSim® v10.2c or later
Xilinx® ISIM 14.6 or later
Xilinx® XST 14.6 or later

Configuration

The DO-254 AXI Interconnect version 1.00a is configurable as shown below:

Settable Parameter	Definition
C_NUM_SLAVE_SLOTS	Number of slave slots
C_NUM_MASTER_SLOTS	Number of master slots
C_FAMILY	Xilinx part family
C_AXI_ID_WIDTH	ID signal width
C_AXI_ADDR_WIDTH	Address signal width
C_S_AXI_IS_INTERCONNECT	Master/AXI interconnect connection
C_INTERCONNECT_DATA_WIDTH	Interconnect data width
C_INTERCONNECT_ACLK_RATIO	Clock frequency ratio
C_AXI_SUPPORTS_USER_SIGNALS	Support user signals
C_AXI_AWUSER_WIDTH	AWUSER signal width
C_AXI_ARUSER_WIDTH	ARUSER signal width
C_AXI_WUSER_WIDTH	WUSER signal width
C_AXI_RUSER_WIDTH	RUSER signal width
C_AXI_BUSER_WIDTH	BUSER signal width
C_AXI_CONNECTIVITY	Connectivity
C_INTERCONNECT_CONNECTIVITY_MODE	Connectivity mode
C_INTERCONNECT_R_REGISTER	Insert register slice on R channel inside interconnect
C_RANGE_CHECK	Range check

Settable Parameter	Definition
Slave Interface	
C_S_AXI_PROTOCOL	AXI protocol
C_S_AXI_DATA_WIDTH	Data width
C_S_AXI_BASE_ID	Base ID
C_S_AXI_THREAD_ID_ WIDTH	Low order ID bits
C_S_AXI_SINGLE_ THREAD	ID thread support
C_S_AXI_ACLK_RATIO	Clock frequency ratio
C_S_AXI_IS_ACLK_ ASYNC	Indicates if SI slot clock is synchronous or asynchronous
C_S_AXI_ARB_ PRIORITY	Arbitration priority
C_S_AXI_WRITE_ ACCEPTANCE	Number of data-active write transactions
C_S_AXI_READ_ ACCEPTANCE	Number of active read transactions
C_S_AXI_SUPPORTS_ WRITE	Indicates whether each SI slot uses Write-related channels
C_S_AXI_SUPPORTS_ READ	Indicates whether each SI slot uses Read-related channels.
C_S_AXI_SUPPORTS_ NARROW_BURST	Indicates whether the connected master device can produce narrow bursts.
C_S_AXI_WRITE_FIFO_ DEPTH	Depth of SI-side Write data FIFO
C_S_AXI_WRITE_FIFO_ DELAY	Packet FIFO write behavior
C_S_AXI_READ_FIFO_ DEPTH	Depth of SI-side Read data FIFO
C_S_AXI_READ_FIFO_ DELAY	Packet FIFO read behavior
C_S_AXI_AW_ REGISTER	Insert register slice on AW channel
C_S_AXI_AR_REGISTER	Insert register slice on AR channel
C_S_AXI_W_REGISTER	Insert register slice on W channel
C_S_AXI_R_REGISTER	Insert register slice on R channel
C_S_AXI_B_REGISTER	Insert register slice on B channel
Master Interface	
C_M_AXI_PROTOCOL	AXI protocol
C_M_AXI_DATA_ WIDTH	Data width
C_M_AXI_BASE_ADDR	Base address
C_M_AXI_HIGH_ADDR	High address of each range
C_M_AXI_ACLK_RATIO	Clock frequency ratio
C_M_AXI_IS_ACLK_ ASYNC	Indicates if MI slot clock is synchronous or asynchronous
C_M_AXI_SUPPORTS_ WRITE	Indicates whether each MI slot uses Write-related channels.
C_M_AXI_SUPPORTS_ READ	Indicates whether each MI slot Read-related channels.
C_M_AXI_WRITE_ ISSUING	Number of data-active Write transactions
C_M_AXI_READ_ ISSUING	Number of active Read transactions
C_M_AXI_SECURE	Indicates whether each MI slot connects to a secure slave device

Settable Parameter	Definition
C_M_AXI_SUPPORTS_NARROW_BURST	Indicates whether the connected slave device is configured to support bursts
C_M_AXI_WRITE_FIFO_DEPTH	Depth of MI-side Write data FIFO
C_M_AXI_WRITE_FIFO_DELAY	Packet FIFO write behavior
C_M_AXI_READ_FIFO_DEPTH	Depth of MI-side Read data FIFO
C_M_AXI_READ_FIFO_DELAY	Packet FIFO read behavior
C_M_AXI_AW_REGISTER	Insert register slice on AW channel
C_M_AXI_AR_REGISTER	Insert register slice on AR channel
C_M_AXI_W_REGISTER	Insert register slice on W channel
C_M_AXI_R_REGISTER	Insert register slice on R channel
C_M_AXI_B_REGISTER	Insert register slice on B channel

Assumptions

Assumption 1: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system/safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.

Assumption 2: The objectives, activities and lifecycle data related specifically to the DO-254 AXI Interconnect Core will be provided to the Integrator for inclusion into their overall certification package.

Assumption 3: Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

Assumption 4: All objectives related to the building, integration and production (including Production Testing — ATP) of the system/LRU will be the responsibility of the integrator.

Assumption 5: Objectives related to hardware components other than the DO-254 AXI Interconnect Core are the responsibility of the integrator.

Assumption 6: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 AXI Interconnect Core in their system.

Assumption 7: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 AXI Interconnect Core.

Assumption 8: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 AXI Interconnect Core into their system.

Assumption 9: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements

to the System/Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 AXI Interconnect Core at the system level.

Assumption 10: The integrator is required to include a clock timing constraint for this DO-254 AXI Interconnect Core. This clock timing constraint will define the clock rate at which the IP core will operate. It is recommended that the integrator defines this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An example UCF file will be provided in Chapter 3 of the 10101-UG, but it is for reference only.

Assumption 11: The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results indicate that all configurations required to attain 100% coverage are tested.

Assumption 12: Some testing of the DO-254 AXI Interconnect Core was done on a test board, the integrator is responsible for complete IP black box testing in his system. ***In order to accomplish this black box testing, the integrator is recommended to design his PCB to have access to at least XX (number defined in 10101-UG) spare FPGA pins that can be connected to a logic analyzer.*** If the integrator chooses to do post place and route simulation on their system as an additional validation, Logicircuit will provide the necessary files for the DO-254 AXI Interconnect Core.

Revision History

Revision	Reason/Description	Date	Subversion repository revision
-	Initial Release	9/2/2014	131