General Description

The AXI 7 Series DDRx (Limited) DO-254 Certifiable Data Package is made up of the artifacts produced by applying the DO-254 lifecycle to the Xilinx® AXI 7 Series DDRx IP v1.07a and an encrypted version of the source code. This includes the following completed documents:

- Plan for Hardware Aspects of Certification
- Hardware Validation and Verification Plan
- Hardware Configuration Management Plan
- Hardware Design Plan
- Hardware Process Assurance Plan
- Hardware Validation and Verification Standard
- Hardware Requirements Standard
- Hardware Design Standard
- Hardware Requirements Document
- Hardware Design Document
- Hardware Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
- Verification Configuration Index
- Hardware Test Procedures
- Hardware Verification Results
- Hardware Elemental Analysis Results
- Hardware Requirements Traceability Matrix
- Hardware Accomplishment Summary

The above documents are available for certification efforts, however not all documents are included in the delivery package.

The DO-254 AXI 7 Series DDRx (Limited) IP Core 1.00a, created and designed by Logicircuit, is a combined pre-engineered controller and physical layer (PHY) for interfacing 7 series FPGA user designs and AMBA® advanced extensible interface (AXI4) slave interfaces to DDR3 and DDR2 SDRAM devices.

This version of the DO-254 AXI 7 Series DDRx (Limited) IP includes the following built-in safety features:

- Error Correcting Code (ECC), for DDR3 memories with 72 bits data width.

Features

- 8-bank support
- 8-word burst support
- 4:1 and 2:1 memory to FPGA logic interface clock ratio
- On-die termination (ODT) support
- I/O Power Reduction option reduces average I/O power by automatically disabling DQ/DQS IBUFs and internal terminations during writes and periods of inactivity
- Two controller request processing modes:
    - Normal: reorder requests to optimize system throughput and latency
    - Strict: memory requests are processed in the order received

DDR3 SDRAM specific features:

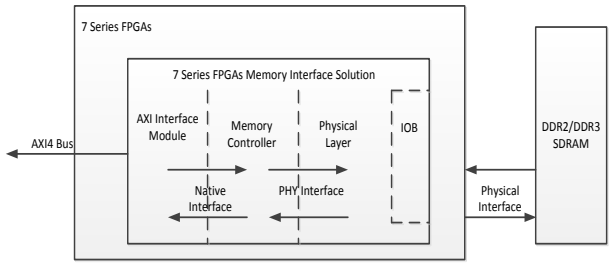
- ECC support
- Configurable data bus widths (doubles from 8, up to 72 bits)
- Support for 5 to 13 cycles of column-address strobe (CAS) latency (CL)
- Support for 5 to 9 cycles of CAS write latency

- JEDEC-compliant DDR3 initialization support

DDR2 SDRAM specific features:

- Component support for interface widths up to 64 bits (ECC is not available in DDR2 memories)
- Configurable data bus widths (doubles from 8, up to 64 bits)
- Support for 3 to 5 cycles of column address strobe (CAS) latency
- JEDEC-compliant DDR2 initialization support

Block Diagram



Supported FPGA Families

Xilinx® 7-Series

Development Tools

Xilinx® ISE/EDK® 14.4 or later
ModelSim® v10.1c or later
Xilinx® ISIM 14.4 or later
Xilinx® XST 14.4 or later

Configuration

The DO-254 AXI 7 Series DDRx (Limited) 1.00a is configurable as shown below:

Parameter Name	Description
C_ADDR_CMD_MODE	This parameter is used by the controller to calculate timing on the memory addr/cmd bus.
C_BANK_WIDTH	Memory bank address bus width.
C_BM_CNT_WIDTH	This is the number of bits required to index a bank machine and is given by ceil(log2(nBANK_MACHS)).
C_BURST_MODE	This is the memory data burst length.
C_BURST_TYPE	This is an option for the ordering of accesses within a burst.
C_CK_WIDTH	This is the number of CK/CK# outputs to memory.
C_CL	This is the read CAS latency. The available option is frequency dependent in the MIG tool.
C_COL_WIDTH	This is the number of memory column address bits.
C_CMD_PIPE_PLUS1	This adds pipeline stage between MC and PHY.

Parameter Name	Description
C_CS_WIDTH	This is the number of unique CS outputs to memory.
C_CKE_WIDTH	This is the number of CKE outputs to memory.
C_CWL	This is the write CAS latency. The available option is frequency dependent in the MIG tool.
C_DATA_BUF_ADDR_WIDTH	This is the bus width of the request tag passed to the memory controller. This parameter is set to 5 for 4:1 mode and 4 for 2:1 mode.
C_PHY_CONTROL_MASTER_BANK	This is the bank number where master PHY_CONTROL resides
C_DDR2_DQSN_ENABLE	This enables differential DQS for DDR2.
C_DM_WIDTH	This is the number of data mask bits.
C_DQ_WIDTH	This is the memory DQ bus width.
C_DQS_WIDTH	This is the memory DQS bus width.

Parameter Name	Description
C_DRAM_TYPE	This is the supported memory standard for the memory controller.
C_DRAM_WIDTH	This is the DQ bus width per DRAM component.
C_ECC	This is the error correction code, available in 72-bit data width configurations.
C_ECC_TEST	This feature is not available.
C_NBANK_MACHS	This is the number of bank machines. A given bank machine manages a single DRAM bank at any given time.
C_NCK_PER_CLK	This is the number of memory clocks per clock.
C_NCS_PER_RANK	This is the number of unique CS outputs per rank for the PHY.
C_ORDERING	This option reorders received requests to optimize data throughput and latency.

Parameter Name	Description
C_IODELAY_HP_MODE	This option enables or disables the IDELAY high-performance mode.
C_BANK_TYPE	IO bank type.
C_DATA_IO_PRIM_TYPE	Primitive type for IO bank.
C_IODELAY_GRP	Design implementation constraint.
C_OUTPUT_DRV	This is the DRAM reduced output drive option.
C_REG_CTRL	This is the option for DIMM or unbuffered DIMM selection.
C_RTT_NOM	This is the nominal ODT value. The “DISABLED” choice cannot be configured in the MIG GUI, and can only be set in the MHS file.
C_RTT_WR	This is the dynamic ODT write termination used in multiple-RANK designs. For single-component designs, RTT_WR should be disabled.

Parameter Name	Description
C_TCK	This is the memory tCK clock period (ps).
C_TCKE	This is the CKE minimum pulse.
C_TFAW	This is the minimum interval of four active commands.
C_TPRDI	This is the periodic read.
C_TRAS	This is the minimum ACTIVE-to-PRECHARGE period for memory.
C_TRCD	This is the ACTIVE-to-READ or – WRITE command delay.
C_TREFI	This is the average periodic refresh interval for memory.
C_TRFC	This is the REFRESH-to-ACTIVE or REFRESH-to-REFRESH command interval.
C_TRP	This is the PRECHARGE command period.
C_TRRD	This is the ACTIVE-to-ACTIVE minimum command period.

Parameter Name	Description
C_TRTP	This is the READ-to-PRECHARGE command delay.
C_TWTR	This is the WRITE-to-READ command delay.
C_TZQI	This is the timing window to perform the ZQCL command in DDR3 SDRAM.
C_TZQCS	This is the timing window to perform the ZQCS command in DDR3 SDRAM.
C_CAL_WIDTH	This is the calibration width.
C_RANKS	This is the number of ranks.
C_ODT_WIDTH	This is the number of ODT outputs to memory.
C_ROW_WIDTH	This is the DRAM component address bus width.
C_BYTE_LANES_B0	Defines the byte lanes being used in a given I/O bank. A “1” in a bit position indicates a byte lane is used, and a “0” indicates unused.

Parameter Name	Description
C_BYTE_LANES_B1	Defines the byte lanes being used in a given I/O bank. A “1” in a bit position indicates a byte lane is used, and a “0” indicates unused.
C_BYTE_LANES_B2	Defines the byte lanes being used in a given I/O bank. A “1” in a bit position indicates a byte lane is used, and a “0” indicates unused.
C_BYTE_LANES_B3	Defines the byte lanes being used in a given I/O bank. A “1” in a bit position indicates a byte lane is used, and a “0” indicates unused.
C_BYTE_LANES_B4	Defines the byte lanes being used in a given I/O bank. A “1” in a bit position indicates a byte lane is used, and a “0” indicates unused.

Parameter Name	Description
C_DATA_CTL_B0	Defines mode of use of byte lanes in a given I/O bank. A “1” in a bit position indicates a byte lane is used for data, and a “0” indicates it is used for address/control.
C_DATA_CTL_B1	Defines mode of use of byte lanes in a given I/O bank. A “1” in a bit position indicates a byte lane is used for data, and a “0” indicates it is used for address/control.
C_DATA_CTL_B2	Defines mode of use of byte lanes in a given I/O bank. A “1” in a bit position indicates a byte lane is used for data, and a “0” indicates it is used for address/control.

Parameter Name	Description
C_DATA_CTL_B3	Defines mode of use of byte lanes in a given I/O bank. A “1” in a bit position indicates a byte lane is used for data, and a “0” indicates it is used for address/control.
C_DATA_CTL_B4	Defines mode of use of byte lanes in a given I/O bank. A “1” in a bit position indicates a byte lane is used for data, and a “0” indicates it is used for address/control.
C_PHY_0_BITLANES	12-bit parameter per byte lane used to determine which I/O locations are used to generate the necessary PHY structures. This parameter is provided as per bank. Except CKE, ODT, and RESET pins, all Data and Address/Control pins are considered for this parameter generation.

Parameter Name	Description
C_PHY_1_BITLANES	12-bit parameter per byte lane used to determine which I/O locations are used to generate the necessary PHY structures. This parameter is provided as per bank. Except CKE, ODT, and RESET pins, all Data and Address/Control pins are considered for this parameter generation.
C_PHY_2_BITLANES	12-bit parameter per byte lane used to determine which I/O locations are used to generate the necessary PHY structures. This parameter is provided as per bank. Except CKE, ODT, and RESET pins, all Data and Address/Control pins are considered for this parameter generation.

Parameter Name	Description
C_CK_BYTE_MAP	Bank and byte lane location information for the CK/CK#. An 8-bit parameter is provided per pair of signals.
C_ADDR_MAP	Bank and byte lane position information for the address. 12-bit parameter provided per pin.
C_BANK_MAP	Bank and byte lane position information for the bank address.
C_CAS_MAP	Bank and byte lane position information for the CAS command.
C_CKE_MAP	Bank and byte lane position information for the Clock Enable.
C_ODT_MAP	Bank and byte lane position information for the On-Die Termination.
C_CKE_ODT_AUX	This enables the aux_out signal.

Parameter Name	Description
C_CS_MAP	Bank and byte lane position information for the chip select. 1 2-bit parameter provided per pin.
C_PARITY_MAP	Bank and byte lane position information for the parity bit. Parity bit exists for RDIMMs only.
C_RAS_MAP	Bank and byte lane position information for the RAS command.
C_WE_MAP	Bank and byte lane position information for the WE command.
C_DQS_BYTE_MAP	Bank and byte lane position information for the strobe.
C_DATA0_MAP	Bank and byte lane position information for the data bus.
C_DATA1_MAP	Bank and byte lane position information for the data bus.
C_DATA2_MAP	Bank and byte lane position information for the data bus.

Parameter Name	Description
C_DATA3_MAP	Bank and byte lane position information for the data bus.
C_DATA4_MAP	Bank and byte lane position information for the data bus.
C_DATA5_MAP	Bank and byte lane position information for the data bus.
C_DATA6_MAP	Bank and byte lane position information for the data bus.
C_DATA7_MAP	Bank and byte lane position information for the data bus.
C_DATA8_MAP	Bank and byte lane position information for the data bus.
C_DATA9_MAP	Bank and byte lane position information for the data bus.
C_DATA10_MAP	Bank and byte lane position information for the data bus.
C_DATA11_MAP	Bank and byte lane position information for the data bus.

Parameter Name	Description
C_DATA12_MAP	Bank and byte lane position information for the data bus.
C_DATA13_MAP	Bank and byte lane position information for the data bus.
C_DATA14_MAP	Bank and byte lane position information for the data bus.
C_DATA15_MAP	Bank and byte lane position information for the data bus.
C_DATA16_MAP	Bank and byte lane position information for the data bus.
C_MASK0_MAP	Bank and byte lane position information for the data mask.
C_MASK1_MAP	Bank and byte lane position information for the data mask.
C_SLOT_0_CONFIG	This is the rank mapping for slot 1.
C_SLOT_1_CONFIG	This is the rank mapping for slot 2.
C_MEM_ADDR_ORDER	This is the memory address order.

Parameter Name	Description
C_SIM_BYPASS_INIT_CAL	This simulation only parameter is used to speed up simulations.
C_REFCLK_FREQ	This is the reference clock frequency for IODELAYCTRLs. This can be set to 200.0 for any speed grade device.
C_USE_CS_PORT	This enables the use of the CS port.
C_USE_DM_PORT	This is the enable data mask option used during memory write operations.
C_USE_ODT_PORT	This enables the use of the ODT port. This parameter cannot be configured in the MIG GUI, and can only be set in the MHS file. Defaults to 1.
C_USE_EXTERNAL_XADC	This instantiates or uses external XADC. This parameter cannot be configured in the MIG GUI, and can only be set in the MHS file. Defaults to 0.

Parameter Name	Description
C_USE_EXTERNAL_IODELAY_CTRL	This enables “iodelay_ctrl_rdy_i” when set to 1.
C_S_AXI_ID_WIDTH	This is the width of ID signals for every channel. This value is automatically computed in EDK designs. This parameter cannot be configured in the MIG GUI, and can only be set in the MHS file. Defaults to 4.
C_S_AXI_ADDR_WIDTH	This is the width of address read and address write signals. EDK designs are limited to 32.
C_S_AXI_DATA_WIDTH	This is the width of data signals. The recommended width is 8x the memory data width. The width can be smaller, but not greater than 8x the memory data width.

Parameter Name	Description
C_S_AXI_SUPPORTS_NARROW_BURST	This parameter adds logic blocks to support narrow AXI transfers. It is required if any master connected to the memory controller issues narrow bursts. This parameter is automatically set if the AXI data width is smaller than the recommended value.
C_RD_WR_ARB_ALGORITHM	This parameter indicates the Arbitration algorithm scheme.
C_S_AXI_REG_EN0	This parameter instantiates register slices before upsizer.
C_S_AXI_REG_EN1	This parameter instantiates register slices after upsizer.

Parameter Name	Description
C_S_AXI_HIGHADDR	This parameter specifies the high address for the memory mapped slave interface. Address requests received above this value wrap back to the base address. The base/high address together defines the accessible size of the memory. This accessible size must be a power of 2. Additionally, the base/high address pair must be aligned to a multiple of the accessible size. The minimum accessible size is 4096 bytes.
C_S_AXI_CTRL_ADDR_WIDTH	This parameter specifies the width of AXI 4 Lite address bus.
C_S_AXI_CTRL_DATA_WIDTH	This parameter specifies the width of AXI 4 Lite data buses.

Parameter Name	Description
C_S_AXI_HIGHADDR	This parameter specifies the high address for the memory mapped slave interface. Address requests received above this value wrap back to the base address. The base/high address together define the accessible size of the memory. This accessible size must be a power of 2. Additionally, the base/high address pair must be aligned to a multiple of the accessible size. The minimum accessible size is 4096 bytes.
C_S_AXI_CTRL_ADDR_WIDTH	This parameter specifies the width of AXI 4 Lite address bus.
C_S_AXI_CTRL_DATA_WIDTH	This parameter specifies the width of AXI 4 Lite data buses.

Parameter Name	Description
C_ECC_ONOFF_RESET_VALUE	This parameter specifies the ECC on/off value at startup/reset. This parameter cannot be configured in the MIG GUI, and can only be set in the MHS file. Defaults to 1.

Assumptions

Assumption 1: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system/safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.

Assumption 2: The objectives, activities and lifecycle data related specifically to the DO-254 AXI 7 Series DDRx (Limited) Core will be provided to the Integrator for inclusion into their overall certification package.

Assumption 3: Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

Assumption 4: All objectives related to the building, integration and production (including Production Testing — ATP) of the system/LRU will be the responsibility of the integrator.

Assumption 5: Objectives related to hardware components other than the DO-254 AXI 7 Series DDRx (Limited) Core are the responsibility of the integrator.

Assumption 6: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 AXI 7 Series DDRx (Limited) Core in their system.

Assumption 7: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 AXI 7 Series DDRx (Limited) Core.

Assumption 8: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 AXI 7 Series DDRx (Limited) Core into their system.

Assumption 9: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System/Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 AXI 7 Series DDRx (Limited) Core at the system level.

Assumption 10: The integrator is required to include a clock timing constraint for this DO-254 AXI 7 Series DDRx (Limited) Core. This clock timing constraint will define the clock rate at

which the IP core will operate. It is recommended that the integrator defines this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An example UCF file will be provided in Chapter 3 of the 10116-UG, but it is for reference only.

Assumption 11: The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results indicate that all configurations required to attain 100% coverage are tested.

Assumption 12: Some testing of the DO-254 AXI 7 Series DDRx (Limited) Core was done on a test board, the integrator is responsible for complete IP black box testing in his system. ***In order to accomplish this black box testing, the integrator is recommended to design his PCB to have access to at least XX (number defined in 10116-UG) spare FPGA pins that can be connected to a logic analyzer.*** If the integrator chooses to do post place and route simulation on their system as an additional validation, Logicircuit will provide the necessary files for the DO-254 AXI 7 Series DDRx (Limited) Core.

Revision History

Revision	Reason/Description	Date	Subversion repository revision
-	Initial Release	08/29/2014	134