LOGICIRCUIT

DO-254 ARINC 429 Transceiver/Receiver Core 1.00a Certifiable Data Package (DAL A)

August 27, 2014, Revision -

General Description

The ARINC 429 Transceiver/Receiver Core DO-254 Certifiable Data Package is made up of the artifacts produced by applying the DO-254 lifecycle to the core and an encrypted version of the source code. This includes the following completed documents:

- Plan for Hardware Aspects of Certification
- Hardware Validation and Verification Plan
- Hardware Configuration Management Plan
- Hardware Design Plan
- Hardware Process Assurance Plan
- Hardware Validation and Verification Standard
- Hardware Requirements Standard
- Hardware Design Standard
- Hardware Requirements Document
- Hardware Design Document
- Hardware Elemental Analysis Results
- Hardware Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
- Verification Configuration Index
- Hardware Test Procedures
- Hardware Verification Results
- Hardware Requirements Traceability Matrix
- Hardware Accomplishment Summary

The above documents are available for certification efforts, however not all documents are included in the delivery package.

The DO- ARINC 429 Transceiver/Receiver Core 1.00a, consists of a separate transmitter and receiver IP core implementing a point to multipoint communication channel bus. The ARINC 429 Receiver With FIFO is capable of decoding high-speed or low-speed messages with or without parity checking.

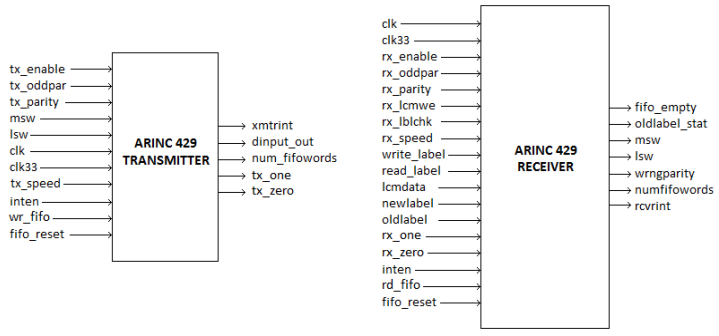
The ARINC 429 Transmitter With FIFO is capable of sending high-speed or low-speed messages with or without a parity bit. There is a FIFO capable of storing up to eight messages while they await transmission.

This version of the DO-254 ARINC 429 Transceiver/Receiver IP Core 1.00a supports data parity error checking to ensure data integrity. The receiver discards data and sets “wrngparity” when a parity error is detected.

Features

- Implements an ARINC 429 point to multipoint communication channel bus
- Supports high-speed or low-speed messages with or without a parity bit
- Label control matrix in receiver to filter out undesired messages

I/O Overview



Supported FPGA Families

Xilinx® 7-Series and Spartan®-6

Development Tools

Xilinx® ISE® 14.4 or later
ModelSim® v10.1b or later
Xilinx® ISIM 14.4 or later
Xilinx® XST 14.4 or later
Precision Synthesis 2012b or later

Configuration

The DO-254 ARINC 429 Transceiver/Receiver IP Core version 1.00a is configurable as shown below:

Settable Parameter	Definition
C_TX_FIFO_ DEPTH	Specifies the depth of the TX FIFO, where the actual FIFO depth is C_RX_FIFO_DEPTH – 1
C_TX_FIFO_ NUMWORDS_ WIDTH	Specifies the width of the number of 32 bit words, "num_fifowords", output
C_RX_FIFO_ DEPTH	Specifies the depth of the RX FIFO, where the actual FIFO depth is C_RX_FIFO_DEPTH - 1
C_RX_FIFO_ NUMWORDS_W IDTH	Specifies the width of the number of 32 bit words, "numwords", output

Assumptions

Assumption 1: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system/safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.

The objectives, activities and lifecycle data related specifically to the DO-254 ARINC 429 Transceiver/Receiver IP Core will be provided to the Integrator for inclusion into their overall certification package.

Assumption 2: Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

Assumption 3: All objectives related to the building, integration and production (including Production Testing — ATP) of the system/LRU will be the responsibility of the integrator.

Assumption 4: Objectives related to hardware components other than the DO-254 ARINC 429 Transceiver/Receiver IP Core are the responsibility of the integrator.

Assumption 5: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 ARINC 429 Transceiver/Receiver IP Core in their system.

Assumption 6: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 ARINC 429 Transceiver/Receiver IP Core.

Assumption 7: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the

DO-254 ARINC 429 Transceiver/Receiver IP Core into their system.

Assumption 8: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System/Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 ARINC 429 Transceiver/Receiver IP Core at the system level.

Assumption 9: The integrator is required to include a clock timing constraint for this DO-254 ARINC 429 Transceiver/Receiver IP Core. This clock timing constraint will define the clock rate at which the IP core will operate. It is recommended that the integrator defines this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An example UCF file will be provided in Chapter 3 of 15100-UG, but it is for reference only.

Assumption 10: The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results indicate that all configurations required to attain 100% coverage are tested.

Revision History

Revision	Reason/Description	Date	Subversion repository revision
-	Initial Release	9/2/2014	109