General Description

The FIFO Generator DO-254 Certifiable Data Package is made up of the artifacts produced by applying the DO-254 lifecycle to the Xilinx® FIFO Generator IP v10.0 and an encrypted version of the source code. This includes the following completed documents:

- Plan for Hardware Aspects of Certification
- Hardware Validation and Verification Plan
- Hardware Configuration Management Plan
- Hardware Design Plan
- Hardware Process Assurance Plan
- Hardware Validation and Verification Standard
- Hardware Requirements Standard
- Hardware Design Standard
- Hardware Requirements Document
- Hardware Design Document
- Hardware Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
- Verification Configuration Index
- Hardware Test Procedures
- Hardware Verification Results
- Hardware Elemental Analysis Results
- Hardware Requirements Traceability Matrix
- Hardware Accomplishment Summary

The above documents are available for certification efforts, however not all documents are included in the delivery package.

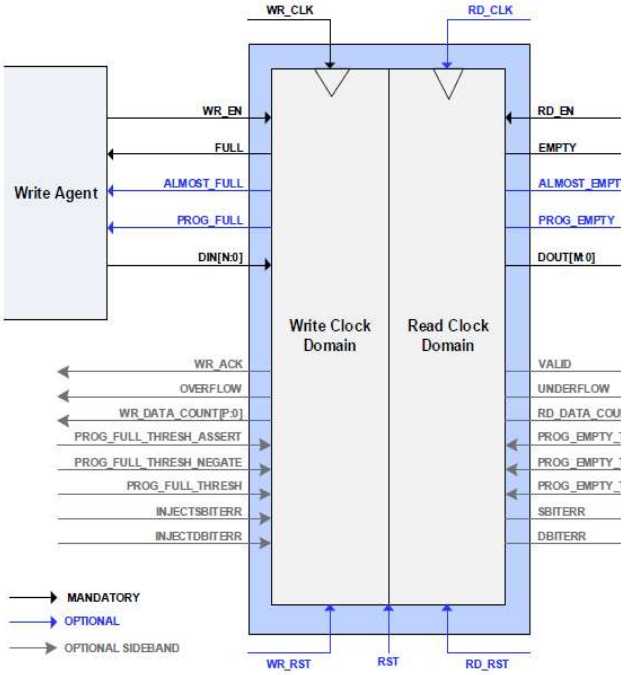
The DO-254 FIFO Generator IP Core 1.00a, created and designed by Logicircuit, is a first-in first-out (FIFO) memory queue for applications requiring in-order storage and retrieval for the Native Interface FIFOs in Xilinx® Field Programmable Gate Arrays (FPGAs).
This version of the DO-254 FIFO Generator IP includes the following built-in safety features:

- Error Correcting Code (ECC), in the 7-Series FPGAs for data widths greater than 64 bits
- Error injection pins in the 7-series FPGAs allow for insertion of single- and double-bit errors
- ECC available for Built-in FIFO and Block memory configurations

Features

- FIFO data widths from 1 to 1024 bits
- Symmetric or Non-symmetric aspect ratios
- Synchronous or asynchronous reset option
- Selectable memory type (block RAM, distributed RAM, or built-in FIFO)
- Full and Empty status flags, and Almost Full and Almost Empty flags for indicating one-word-left
- Programmable Full and Empty flags, set by user-defined constant(s) or dedicated input port(s)
- Hamming Error Injection and Correction Checking (ECC) support for block RAM and Built-In FIFO configurations
- Embedded register option for block RAM and built-in FIFO configurations

Pinout Diagram



Supported FPGA Families

Xilinx® 7-Series and Spartan®-6

Development Tools

Xilinx® ISE/EDK® 14.4 or later
ModelSim® v10.2c or later
Xilinx® ISIM 14.4 or later
Xilinx® XST 14.4 or later

Configuration

The DO-254 FIFO Generator version 1.00a is configurable as shown below:

Settable Parameter	Definition
C_COMMON_CLOCK	• 0: Independent Clock • 1: Common Clock
C_DATA_COUNT_WIDTH	Width of DATA_COUNT bus (1 – 23)
C_DIN_WIDTH	Width of DIN bus (1 – 1024) Width must be > 1 for ECC with Double bit error injection
C_DOUT_RST_VAL	Reset value of DOUT Hexadecimal value, 0 - 'F's equal to C_DOUT_WIDTH
C_DOUT_WIDTH	Width of DOUT bus (1 – 1024) Width must be > 1 for ECC with Double bit error injection
C_ENABLE_RST_SYNC	• 0: Do not synchronize the reset (WR_RST/ • RD_RST is directly used, available only for independent clock) • 1: Synchronize the reset

Settable Parameter	Definition
C_ERROR_INJECTION_TYPE	• 0: No error injection • 1: Single bit error injection • 2: Double bit error injection • 3: Single and double bit error injection
C_FAMILY	Device family (for example, Virtex™-7)
C_FULL_FLAGS_RST_VAL	Full flags rst val (0 or 1)
C_HAS_ALMOST_EMPTY	• 0: Core does not have ALMOST_EMPTY flag • 1: Core has ALMOST_EMPTY flag
C_HAS_ALMOST_FULL	• 0: Core does not have ALMOST_FULL flag • 1: Core has ALMOST_ FULL flag
C_HAS_DATA_COUNT	• 0: Core does not have DATA_COUNT bus • 1: Core has DATA_COUNT bus
C_HAS_OVERFLOW	• 0: Core does not have OVERFLOW flag • 1: Core has OVERFLOW flag
C_HAS_RD_DATA_COUNT	• 0: Core does not have RD_DATA_COUNT bus • 1: Core has RD_DATA_COUNT bus

Settable Parameter	Definition
C_HAS_RST	• 0: Core does not have asynchronous reset (RST) • 1: Core has asynchronous reset (RST)
C_HAS_SRST	• 0: Core does not have synchronous reset (SRST) • 1: Core has synchronous reset (SRST)
C_HAS_UNDERFLOW	• 0: Core does not have UNDERFLOW flag • 1: Core has UNDERFLOW flag
C_HAS_VALID	• 0: Core does not have VALID flag • 1: Core has VALID flag
C_HAS_WR_ACK	• 0: Core does not have WR_ACK flag • 1: Core has WR_ACK flag
C_HAS_WR_DATA_COUNT	• 0: Core does not have WR_DATA_COUNT bus • 1: Core has WR_DATA_COUNT bus 21 C_IMPLEMENTATION_0: Common-Clock Block RAM/Distributed

Settable Parameter	Definition
C_IMPLEMENTATION_TYPE	• 0: Common-Clock Block RAM/Distributed RAM FIFO • 2: Independent Clocks Block RAM/Distributed RAM FIFO • 6: 7 Series Built-In FIFO
C_MEMORY_TYPE	• 1: Block RAM • 2: Distributed RAM • 4: Built-in FIFO
C_MSGON_VAL	• 0: Disables timing violation on cross clock domain registers • 1: Enables timing violation on cross clock domain registers
C_OVERFLOW_LOW	• 0: OVERFLOW active high • 1: OVERFLOW active low
C_PRELOAD_LATENCY	• 0: First-Word Fall-Through with or without Embedded Register • 1: Standard FIFO without Embedded Register • 2: Standard FIFO with Embedded Register
C_PRELOAD_REGS	• 0: Standard FIFO without Embedded Register • 1: Standard FIFO with Embedded Register or First-Word Fall-Through with or without Embedded Register
C_PRIM_FIFO_TYPE	Primitive used to build a FIFO (Ex. “512x36”)
C_PROG_EMPTY_THRESH_ASSERT_VAL	PROG_EMPTY assert threshold[(a)]
C_PROG_EMPTY_THRESH_NEGATE_VAL	PROG_EMPTY negate threshold[(a)]
C_PROG_EMPTY_TYPE	• 0: No programmable empty • 1: Single programmable empty thresh constant • 2: Multiple programmable empty thresh constants • 3: Single programmable empty thresh input • 4: Multiple programmable empty thresh inputs
C_PROG_FULL_THRESH_ASSERT_VAL	PROG_FULL assert threshold[(a)]
C_PROG_FULL_THRESH_NEGATE_VAL	PROG_FULL negate threshold[(a)]

Settable Parameter	Definition
C_PROG_FULL_TYPE	• 0: No programmable full • 1: Single programmable full thresh constant • 2: Multiple programmable full thresh constants • 3: Single programmable full thresh input • 4: Multiple programmable full thresh inputs
C_RD_DATA_COUNT_WIDTH	Width of RD_DATA_COUNT bus (1 – 23)
C_RD_DEPTH	Depth of read interface (16 – 4194304)
C_RD_FREQ	Read clock frequency (1 MHz – 1000 MHz)
C_RD_PNTR_WIDTH	log2(C_RD_DEPTH)
C_UNDERFLOW_LOW	• 0: UNDERFLOW active high • 1: UNDERFLOW active low
C_USE_DOUT_RST	• 0: Does not reset DOUT on RST • 1: Resets DOUT on RST
C_USE_ECC	• 0: Does not use ECC feature • 1: Uses ECC feature
C_USE_EMBEDDED_REG	• 0: Does not use BRAM embedded output register • 1: Uses BRAM embedded output register
C_USE_FWFT_DATA_COUNT	• 0: Does not use extra logic for FWFT data count • 1: Uses extra logic for FWFT data count
C_VALID_LOW	• 0: VALID active high • 1: VALID active low
C_WR_ACK_LOW	• 0: WR_ACK active high • 1: WR_ACK active low
C_WR_DATA_COUNT_WIDTH	Width of WR_DATA_COUNT bus (1 – 23)
C_WR_DEPTH	Depth of write interface (16 – 4194304)
C_WR_FREQ	Write clock frequency (1 MHz – 1000 MHz)
C_WR_PNTR_WIDTH	log2(C_WR_DEPTH)

(a) See the FIFO Generator GUI for the allowable range of values.

Assumptions

Assumption 1: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system/safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.

Assumption 2: The objectives, activities and lifecycle data related specifically to the DO-254 FIFO Generator Core will be provided to the Integrator for inclusion into their overall certification package.

Assumption 3: Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

Assumption 4: All objectives related to the building, integration and production (including Production Testing — ATP) of the system/LRU will be the responsibility of the integrator.

Assumption 5: Objectives related to hardware components other than the DO-254 FIFO Generator Core are the responsibility of the integrator.

Assumption 6: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 FIFO Generator Core in their system.

Assumption 7: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 FIFO Generator Core.

Assumption 8: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 FIFO Generator Core into their system.

Assumption 9: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System/Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 FIFO Generator Core at the system level.

Assumption 10: The integrator is required to include a clock timing constraint for this DO-254 FIFO Generator Core. This clock timing constraint will define the clock rate at which the IP core will operate. It is recommended that the integrator defines this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An example UCF file will be provided in Chapter 3 of the 10123-UG, but it is for reference only.

Assumption 11: The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results indicate that all configurations required to attain 100% coverage are tested.

Assumption 12: Some testing of the DO-254 FIFO Generator Core was done on a test board, the integrator is responsible for complete IP black box testing in his system. ***In order to accomplish this black box testing, the integrator is recommended to design his PCB to have access to at least XX (number defined in 10123-UG) spare FPGA pins that can be connected to a logic analyzer.*** If the integrator chooses to do post place and route simulation on their system as an additional validation, Logicircuit will provide the necessary files for the DO-254 FIFO Generator Core.

Revision History

Revision	Reason/Description	Date	Subversion repository revision
-	Draft 4 has been formally released as Rev. -	6/16/2014	163