## General Description

The AXI4-Lite IP Interface (IPIF) DO-254 Certifiable Data Package is made up of the artifacts produced by applying the DO-254 lifecycle to the Xilinx® AXI4-Lite IPIF IP and an encrypted version of the source code. This includes the following completed documents:

- Plan for Hardware Aspects of Certification
- Hardware Validation and Verification Plan
- Hardware Configuration Management Plan
- Hardware Design Plan
- Hardware Process Assurance Plan
- Hardware Validation and Verification Standard
- Hardware Requirements Standard
- Hardware Design Standard
- Hardware Requirements Document
- Hardware Design Document
- Hardware Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
- Verification Configuration Index
- Hardware Test Procedures
- Hardware Verification Results
- Hardware Elemental Analysis Results
- Hardware Requirements Traceability Matrix
- Hardware Accomplishment Summary

The above documents are available for certification efforts, however not all documents are included in the delivery package.
The AXI4-Lite IP Interface (IPIF) is a part of the Xilinx family of Advanced RISC Machine (ARM®) Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI) control interface compatible products. It provides a point-to-point bidirectional interface between a user Intellectual Property (IP) core and the AXI interconnect. This version of the AXI4-Lite IP Interface (IPIF) has been optimized for slave operation on the AXI.

## Safety Features

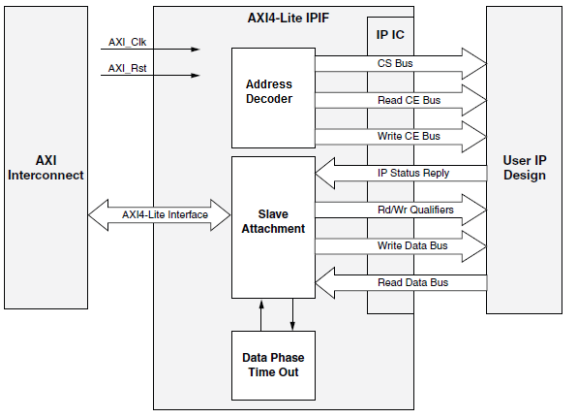
This version of the Xilinx® LMB IP has the following built-in safety features

- IP error indication signal Bus2IP_error

## Features

- Supports 32-bit slave configuration
- Supports read and write data transfers of 32-bit width
- Supports multiple address ranges
- Read has the higher priority over write
- Both the AXI and IP Interconnect (IPIC) are little endian

## Block Diagram




### Supported FPGA Families

Xilinx® 7-Series, Spartan®-6 and Ultrascale™

## Development Tools

Xilinx® EDK® 14.4 or later
ModelSim® v10.2a or later
Xilinx® ISIM 14.4 or later
Xilinx® XST 14.4 or later
Xilinx® Vivado® 2015.3 or later

## Configuration

The DO-254 AXI4-Lite IPIF is configurable as shown below:

| Settable Parameter | Allowable Values |
|---|---|
| C_FAMILY | Spartan-6 and 7-series families |
| C_USE_WSTRB[1] | 0, 1 |
| C_DPHASE_TIMEOUT | 0 to 512[4] |
| C_S_AXI_ADDR_WIDTH | 32 |
| C_S_AXI_DATA_WIDTH | 3-32 |
| C_S_AXI_MIN_SIZE | Valid range[2] |
| C_ARD_ADDR_RANGE_ ARRAY | An array containing pairs of valid 32-bit addresses.[3] |
| C_ARD_NUM_CE_ARRAY | An array of positive integers that are powers of 2.[3] |

Notes:

(1) If the C_USE_WSTRB = 0, the Bus2IP_BE = "1111". Otherwise Bus2IP_BE = S_AXI_WSTRB.
(2) The C_S_AXI_MIN_SIZE indicates the minimum size of the address space required by the IP. The min size of the address space is IP specific and must be a power of 2 - 1.
(3) The arrays in C_ARD_NUM_CE_ARRAY and C_ARD_ADDR_RANGE_ARRAY must contain the same number of entries.
(4) The values will be rounded up to a power of 2.

## Assumptions

**Assumption 1**: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system / safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.

**Assumption 2**: The objectives, activities and lifecycle data related specifically to the DO-254 AXI4-Lite IPIF IP Core will be provided to the Integrator for inclusion into their overall certification package.

**Assumption 3**: Place and route, clock frequency, and parameter selection decisions related to the IP core will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

**Assumption 4**: All objectives related to the building, integration and Production (including Production Testing - ATP) of the system/LRU will be the responsibility of the integrator.

**Assumption 5**: Objectives related to hardware components other than the DO-254 AXI4-Lite IPIF IP Core are the responsibility of the integrator.

**Assumption 6**: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 AXI4-Lite IPIF IP Core in their system.

**Assumption 7**: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 AXI4-Lite IPIF IP Core.

**Assumption 8**: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 AXI4-Lite IPIF IP Core into their system.

**Assumption 9**: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System / Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 AXI4-Lite IPIF IP Core at the system level.

**Assumption 10**: The integrator is required to include a clock timing constraint for this DO-254 AXI4-Lite IPIF IP Core. This clock timing constraint will define the clock rate at which the IP core will operate. It is recommended that the integrator defines this constraint in the UCF file. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc. An example UCF file will be provided in Chapter 3 of the 10112-UG, but it is for reference only.

**Assumption 11:** The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results indicate that all configurations required to attain 100% coverage are tested.

**Assumption 12:** Some testing of the DO-254 AXI4-Lite IPIF IP Core was done on a test board, the integrator is responsible for complete IP black box testing in his system. ***In order to accomplish this black box testing, the integrator is recommended to design his PCB to have access to at least XX (number defined in 10112-UG) spare FPGA pins that can be connected to a logic analyzer.*** If the integrator chooses to do post place and route simulation on their system as an additional validation, Logicircuit will provide the necessary files for the DO-254 AXI4-Lite IPIF IP Core.

## Revision History

| Revision | Reason/Description | Date | Subversion repository revision |
|---|---|---|---|
| - | Draft2 has been formally released as Rev. - | 12/12/2012 | 163 |
| A | PR_030_0032<br>PR_030_0033 | 10/22/2013 | 154 |
| B | PR_030_0045 | 4/29/2016 | 236 |