General Description

The DO-254 AXI SmartConnect IP Core Certifiable Data Package (CDP) is made up of the artifacts produced by applying the DO-254 lifecycle to the Xilinx® AXI SmartConnect IP, v1.0, (as defined in Xilinx PG247 LogiCORE IP AXI SmartConnect IP (v1.0) Product Guide Rev 1.0, dated 19 October, 2022), and an encrypted version of the source code. This includes the following completed documents:

- Plan for Hardware Aspects of Certification
- Hardware Validation and Verification Plan
- Hardware Configuration Management Plan
- Hardware Design Plan
- Hardware Process Assurance Plan
- Hardware Validation and Verification Standard
- Hardware Requirements Standard
- Hardware Design Standard
- Hardware Requirements Document
- Hardware Design Document
- Hardware Configuration Index
- Verification Configuration Index (includes Hardware Lifecycle Environment Configuration Index)
- Hardware Test Procedures
- Hardware Verification Results
- Hardware Elemental Analysis Results
- Hardware Requirements Traceability Matrix
- Hardware Accomplishment Summary

The above documents are available for certification efforts, however not all documents are included in the delivery package.

The DO-254 AXI SmartConnect is an AXI slave IP used to connect one or more AXI memory-mapped master devices to one or more memory-mapped slave devices. The DO-254 AXI SmartConnect IP Core is validated to operate with 1 connected AXI4 Master, and 4 connected AXI4-Lite Slaves.

For I/Os, specifics on allowable configurations, and any discrepancies versus the Xilinx PG247 Product Specification, please see the 10159-UG.

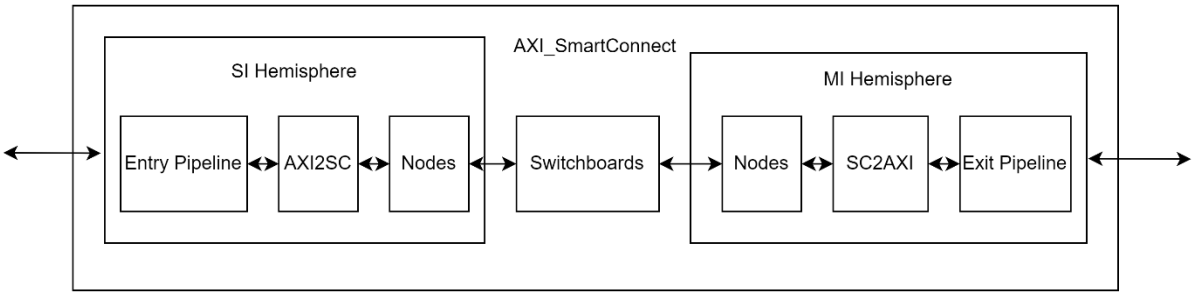
Features

- 1 Slave Interface (SI) and 4 Master Interfaces (MIs) per instance.
- AXI Protocol compliant. Each SI can be connected to a master of type AXI4, and each MI can be connected to a slave of type AXI4-Lite.
- Transactions between interfaces of different protocol types are automatically converted by SmartConnect.
- Burst transactions are automatically split, as required, to remain AXI compliant.
- Interface Data Widths (bits):
  - AXI4: 64.
  - AXI4-Lite: 32.
- Transactions between interfaces of different data widths are automatically converted by SmartConnect.
- Address width: 32-bits:
- SmartConnect decodes 4 total address range segments.
- Single data-beat transactions can traverse the SmartConnect at the same bandwidth as multi-beat bursts.
- Internally resynchronized reset:

- One reset input per IP.

Block Diagram

The high-level block diagram for the DO-254 AXI SmartConnect IP Core is shown below:



Supported FPGA Families

- Xilinx® UltraScale+
- Xilinx® UltraScale
- Xilinx® 7-Series

Development Tools

- ModelSim® v10.7g or later
- Xilinx® Vivado® v2022.1 or later

DO-254 IP Dependencies

- DO-254 Xilinx Parameterized Macros (XPM) IP (10140)
- DO-254 Processor System Reset IP (10108)

Assumptions

Assumption 1: The integrator will develop a full set of DO-254 artifacts to reflect the objectives, activities, and lifecycle data related to the system/safety, implementation, target test, acceptance test, production transition aspects, related validation and verification, configuration management, process assurance, and certification liaison aspects of the system/LRU.

Assumption 2: The objectives, activities, and lifecycle data related specifically to the DO-254 AXI SmartConnect IP will be provided to the integrator for inclusion into their overall certification package.

Assumption 3: Place and route, clock frequency, and parameter selection decisions related to the IP will have an impact on critical areas such as timing. These decisions and the verification of these implementation decisions will be the responsibility of the integrator.

Assumption 4: All objectives related to the building, integration, and production (including Production Testing — ATP) of the system/LRU will be the responsibility of the integrator.

Assumption 5: Objectives related to hardware components other than the DO-254 AXI SmartConnect IP are the responsibility of the integrator.

Assumption 6: The integrator will develop all DO-254 artifacts that are related to the integration and testing of the DO-254 AXI SmartConnect IP in their system.

Assumption 7: The integrator will perform implementation objectives related to the target hardware, including the integral process objectives, to verify the timing and other critical parameters of the DO-254 AXI SmartConnect IP.

Assumption 8: The applicant is responsible for communicating with their Certification Authority relative to the implementation of the DO-254 AXI SmartConnect IP into their system.

Assumption 9: Compliance with the objectives related to system (and safety-related) requirements allocated to the hardware will be the responsibility of the integrator. The requirement to feed all IP derived requirements to the System/Safety Process will be the responsibility of the integrator. The integrator will be required to generate hardware requirements allocated from the system requirements that exercise the DO-254 AXI SmartConnect IP at the system level.

Assumption 10: The integrator is required to include a clock timing constraint for this DO-254 AXI SmartConnect IP. This clock timing constraint will define the clock rate at which the IP will operate. It is recommended that the integrator defines this constraint in the XDC file. An example clock constraint which would go in a XDC file will be provided in the User's Guide (10159-UG), but it is for reference only. The integrator typically would also include (at a minimum, but not limited to) pinout constraints, I/O electrical standards, etc.

Assumption 11: The integrator is not required to rerun any elemental analysis (code coverage). Code coverage results indicate that all configurations required to attain 100% coverage are tested.

Assumption 12: Some testing of the DO-254 AXI SmartConnect IP was done on test boards, the integrator is responsible for complete IP black box testing in their system to verify that the IP performs its intended function in the system. In order to assist the integrator with determining what should be tested at the system level, Logicircuit has included a list of potential target tests in the User's Guide (10159-UG). The integrator should evaluate the list of tests against the hardware functions of the IP they are using in their system to determine which tests they should perform at the system level.

Revision History

Revision	Reason/Description	Date	Subversion Repository Revision
-	Initial Release	10/3/2024	19